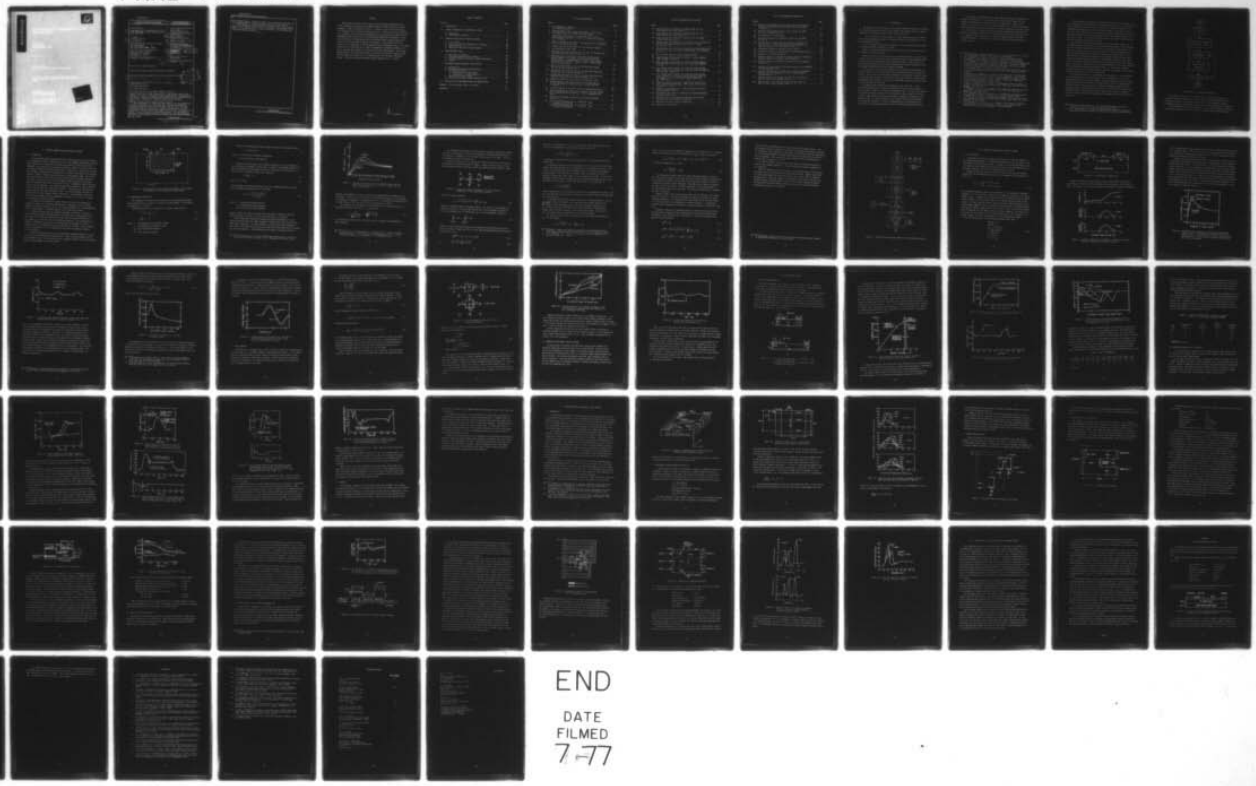
AD-A040 629. RCA LABS PRINCETON N J F/G 9/5
TRANSVERSE TELDS (TRANSFERRED-ELECTRON LOGIC DEVICES).(U)
MAR 77 W R CURTICE N00014-76-C-0465
UNCLASSIFIED PRRL-77-CR-9 NL

| OF |
ADA
040629



END

DATE
FILMED
7-77

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER / 2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): TRANSVERSE TELDs (TRANSFERRED-ELECTRON LOGIC DEVICES).	5. TYPE OF REPORT & PERIOD COVERED: Annual Report (12-1-75 to 11-30-76)
	6. PERFORMING ORG. REPORT NUMBER: PRRL-77-CR-9
7. AUTHOR(s): W. R. Curtice	8. CONTRACT OR GRANT NUMBER(s): N00014-76-C-0465
9. PERFORMING ORGANIZATION NAME AND ADDRESS: RCA Laboratories, Princeton, New Jersey 08540	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: PE 62762N, RF 54-582-001, NR 383-029
11. CONTROLLING OFFICE NAME AND ADDRESS: Office of Naval Research, Department of the Navy, Arlington, VA 22217	12. REPORT DATE: March 1977
	13. NUMBER OF PAGES: 75
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Annual rept. 1 Dec 75-30 Nov 76

18. SUPPLEMENTARY NOTES

ONR Scientific Officer

Tel: (202) 692-4218

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Transferred-Electron Logic Device (TELD); Gunn-Effect Logic Device (GELD); GaAs Logic; Schottky-Barrier Gate/Gunn-Effect Digital Device (SBG·GEDD); Transverse-Domain-Spreading (TDS) Device; Two-Dimensional Semiconductor Simulation; Transient Semiconductor Analysis

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The development of a computer-aided analysis for two-dimensional transient simulations of planar GaAs logic devices utilizing the transferred-electron effect is described. The effects of the semi-insulating substrate, diffusion, a Schottky-barrier gate, and the nonlinearity velocity-field relationship are included. The analysis is applied to two- and three-terminal GaAs devices. The switching properties of three-terminal devices are studied both for anode loading

over

DD FORM 1 JAN 73 1473

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

299 000

20.

and cathode loading. A delay of about 30 ps is obtained with gain for anode loading and for above-threshold-value gate input voltage.

Three designs of transverse-domain-spreading (TDS) logic devices useful for an exclusive-OR circuit are analyzed. The shortest output delay is 20 ps and occurs for a TDS device with a control anode and capacitive output electrode.

PREFACE

This report describes research done in the Microwave Technology Center of RCA Laboratories under Contract Number N00014-76-C-0465 during the period December 1, 1975 to November 30, 1976. F. Sterzer is the Center's Director; S. Y. Narayan was the Project Supervisor and W. R. Curtice the Project Engineer. B. S. Perlman, of the Microwave Technology Center, provided much assistance in implementing the program on the Hewlett-Packard 9600E RTE minicomputer. Likewise F. Brehm of the Integrated Circuit Technology Center assisted greatly in the use of the Data General Eclipse minicomputer. This computer was used courtesy of N. Goldsmith, of the Integrated Circuit Technology Center. The assistance of A. W. Jessup and M. R. Zonis of Management Information Systems in the use of the main RCA computer at Cherry Hill is also acknowledged. The device designs using a Schottky-barrier gate for control of transverse domain spreading are based on the work of L. C. Upadhyayula of the Microwave Technology Center. The Office of Naval Research Project Engineer is M. N. Yoder.

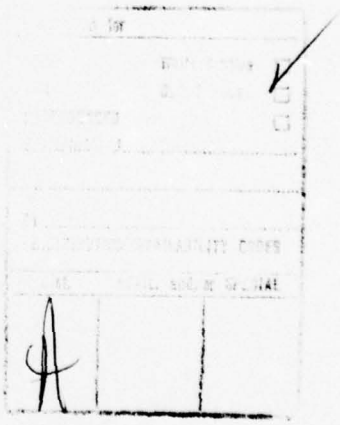


TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

I. INTRODUCTION

The objective of this program is to develop computer simulation techniques for transferred-electron logic devices (TELDs) that employ transverse domain spreading. The specific goals of this year's effort are:

(i) To develop a dynamic model for dipole domain formation in TELDs and to study domain propagation in directions along and perpendicular to the applied electric field.

(ii) To design an optimum configuration for an exclusive-OR gate based on transverse domain spreading in a TELD.

(iii) To develop initial designs for five other logic functions based on transverse domain spreading.

During the course of this program it was deemed necessary to devote substantial effort to the simulation of conventional planar three-terminal TELDs operating in the depletion and quasi-enhancement modes. This was done to provide design support to concurrent ONR-sponsored research programs on TELD development (N00014-76-C-0464 and N00014-75-C-0100).

This phase of our study has resulted in the successful development of a computer program for the two-dimensional transient simulation of planar GaAs devices. The effects of planar ohmic contacts, Schottky-barrier control gate, a semi-insulating substrate, carrier diffusion, and nonlinear velocity-field relationship were studied. The effect of gradually tapering the device width can also be taken into account.

A complete three-dimensional simulation is not practical. A two-dimensional analysis was therefore developed which can be applied either to the top surface plane of a transverse-spreading device or to the plane formed by cutting the device normal to the top surface. These models were used to analyze a wide variety of GaAs logic devices. Numerical calculations were performed both on a large computer and on several different minicomputers. This study has resulted in a better understanding of the properties and application of conventional TELDs as well as transverse-spreading devices.

The earlier, two-dimensional dc transistor simulations by Slotboom [1], Dubock [2], Zaluska et al. [3], Reiser [4], Kennedy and O'Brien [5], and others led eventually to efficient transient simulations. Reiser [6], Suzuki et al. [7], Goto et al. [8], and Yamaguchi et al. [9] have used finite-difference equations to solve the majority carrier problem on a digital computer. The effects of minority carriers in bipolar transistors have been included for transient simulations by Jesshope [10] and by Manck and Engl [11]. J. J. Barnes et al. [12] have used a finite-element method to study the transient behavior of field-effect transistors (FETs), neglecting minority carrier effects.

1. J. W. Slotboom," "Iterative Scheme for 1- and 2-Dimensional D.C. Transistor Insulation," Electron. Lett. 5(26), 677-678 (1969).
2. P. A. Dubock, "D.C. Numerical Model for Arbitrarily Biased Bipolar Transistor in Two Dimensions," Electron. Lett. 6(3), 53-55 (1970).
3. E. J. Zaluska, P. A. Dubock, and H. A. Kemhadjian, "Practical 2-Dimensional Bipolar-Transistor Analysis Algorithm," Electron. Lett. 9(25), 599-600
4. M. Reiser, "Two-Dimensional Analysis of Substrate Effects in Junction F.E.T.'s," Electron. Lett. 6(16), 493-494 (1970).
5. D. P. Kennedy and R. R. O'Brien, "Computer Aided Two-Dimensional Analysis of the Junction Field-Effect Transistor," IBM J. Res. Dev. 14, 95-116 (1970).
6. M. Reiser, "A Two-Dimensional Numerical FET Model for DC, AC and Large Signal Analysis," IEEE Trans. Electron Devices ED-20(1), 35-45 (1973).
7. N. Suzuki, H. Yanai, and T. Ikoma, "Simple Analysis and Computer Simulation on Lateral Spreading of Space Charge in Bulk GaAs," IEEE Trans. Electron Devices ED-19(3), 364-375 (1972).
8. G. Goto, T. Nakamura, and T. Isobe, "Two-Dimensional Domain Dynamics in a Planar Schottky-Gate Gunn-Effect Device," IEEE Trans. Electron Devices ED-22(3), 120-126 (1975).
9. K. Yamaguchi, S. Asai, and H. Kodera, "Two Dimensional Numerical Analysis of Stability Criteria of GaAs FET's," IEEE Trans. Electron Devices ED-23(12), 1283-1290 (1976).
10. C. R. Jesshope, "Numerical Solutions to the 2-Dimensional Time-Dependent Semiconductor Equations," Electron. Lett. 11(18), 431-433 (1975).
11. O. Manck and W. L. Engl, "Two-Dimensional Computer Simulation for Switching a Bipolar Transistor Out of Saturation," IEEE Trans. Electron Devices ED-22(6), 339-347 (1975).
12. J. J. Barnes, R. J. Lomax, and G. I. Haddad, "Finite-Element Simulation of GaAs MESFET's with Lateral Doping Profiles and Submicron Gates," IEEE Trans. Electron Devices ED-23(9), 1042-1048 (1976).

The assumptions, equations, and variables used here are very similar to those employed by Reiser [6] for the silicon FET [except for the velocity-field (v-E) relationship] and by Suzuki et al. [7] for GaAs logic devices. The fundamental variables are the mobile electron density N and the electric potential. These variables are functions of two spatial dimensions and of time. All minority carrier effects are neglected since only majority carrier devices are studied. The finite-difference forms of Poisson's equation and the equation of current continuity are used.

The effects of the intervalley transfer time have been studied, but no convenient method of including these effects has been found. Rees [13] shows that the effective relaxation time of the velocity-field relationship is at least several picoseconds. Hockney and Warriner [14] have analyzed both an FET and a two-terminal TED by using a microscopic-scattering model. This model assumes a two-band approximation for GaAs and includes the important scattering mechanisms which produce the intervalley scattering time. This analysis, however, requires considerably more programming effort and running time. The results differ most for very short devices, such as high-frequency FET structures and millimeter-wavelength TEDs. As the present study is primarily concerned with relatively large devices, the neglect of intervalley transfer time should not cause serious error.

The initial approach to this problem was to develop a computer program for the determination of dc solutions to the two-dimensional problem at a Schottky-barrier-gate GaAs logic device. Poisson's equation and the current continuity equation were solved by iteration until they were simultaneously satisfied within a specified error. Several convergence problem were encountered when device doping densities above $2 \times 10^{15}/cm^3$ were used and also whenever electric fields anywhere in the device were above the threshold value for negative differential mobility. The program flow chart is given in Fig. 1(a).

13. H. D. Rees, "Time Response of the High-Field Electron Distribution Function in GaAs," IBM J. Res. Dev. 13, 537-542 (1969).
14. R. W. Hockney and R. A. Warriner, "Two-Dimensional Particle Models in Semiconductor-Device Analysis," Electron. Lett. 13(23), 484-486 (1974).

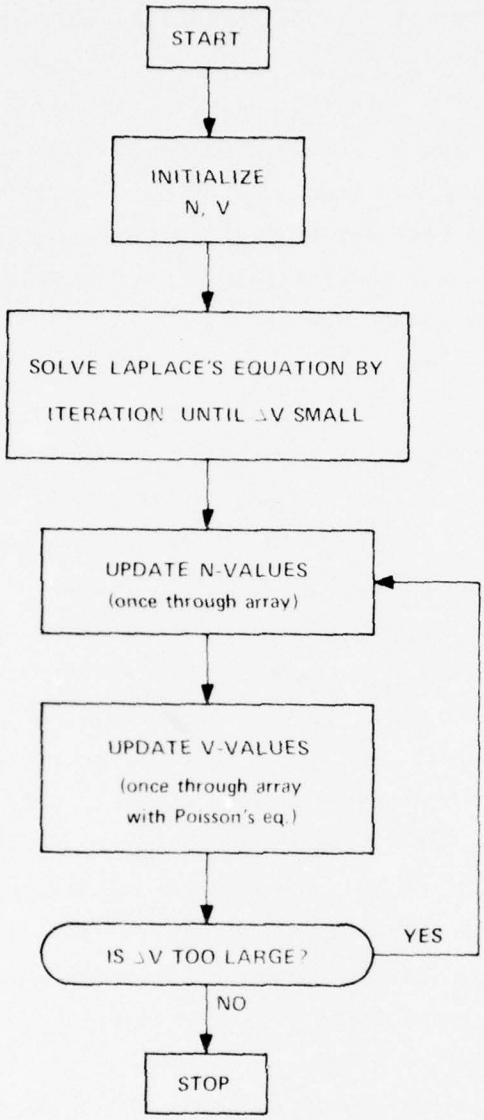


Figure 1(a). Steady-state analysis.

By changing each step for updating N into a physical time step, and iterating Poisson's equation, the steady-state program was converted into a time-domain analysis, illustrated in Fig. 1(b). The time-domain analysis has proven to be the most efficient form, also for the solution of dc problems.

The time-domain analysis is applicable to ac problems, transient problems, large-signal problems, and dc problems; dc problems are handled by running

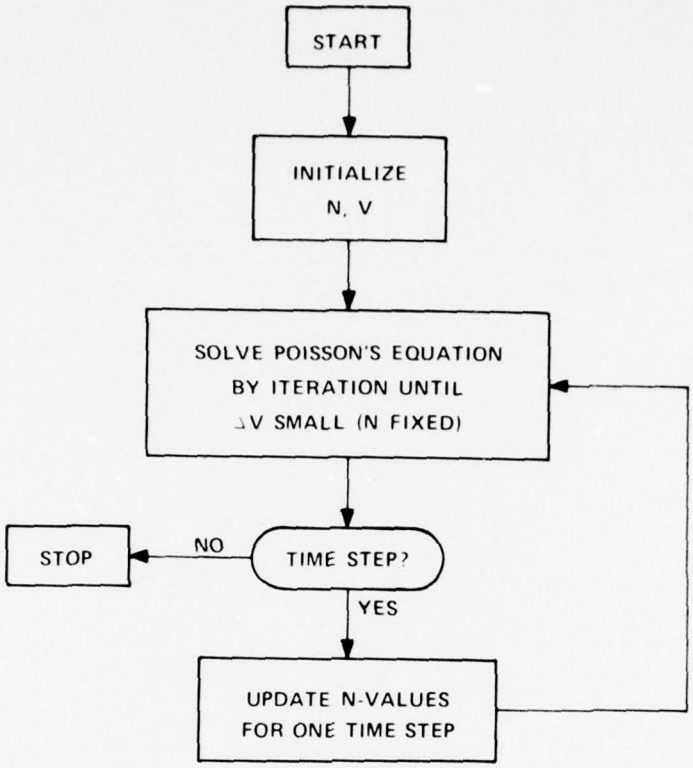


Figure 1(b). Transient analysis.

solutions until all transients have died out. As long as the time step is properly chosen, numerical stability problems should not occur for any of these cases. In addition, as Reiser [6] has shown, the transient behavior of a device can be used to evaluate its ac equivalent circuit.

Only limited investigation was made of the accuracy of the solutions. The principal check on accuracy was made by an independent calculation of total current flow across various planes of the device. The current must be the same for two planes anywhere between two electrodes. Also, the total current flow into the device through all electrodes must be zero. These conditions are checked at every tenth time step; if these current conservation rules are not upheld, calculations are stopped.

The general formulation of the two-dimensional model is presented in Section II. The validity of the analysis is checked by evaluation of the

properties of planar, two-terminal devices in Section III. Section IV presents the study of properties of three-terminal, Schottky-barrier-gate TELDs. Section V describes the results of a study of transverse-domain-spreading (TDS) devices. Conclusions and recommendations are given in Section VI.

II. GENERAL FORMULATION OF MATHEMATICAL MODEL

A. ASSUMPTIONS

The two-dimensional transient analysis of GaAs devices has been developed as a program for digital computation by use of the FORTRAN programming language. Only electrons are considered, Cartesian coordinates are used, and carrier transport is described by the diffusion equations, wherein the finite time for intervalley transfer for electrons in GaAs is neglected. A section of the GaAs device under consideration is divided into an array of mesh points with uniform spacing. Figure 2 shows an array used for a three-terminal TELD. The bottom and the two sides of this array are arbitrarily chosen far enough away from the region of interest so as to have minimal effect upon device solutions. Figure 2 indicates that the actual device chip is considerably larger than the region used for analysis. The boundary conditions assumed are that no electric flux or carrier flow can cross these surfaces. This means that the electric field normal to such free surfaces is zero. The same boundary condition is applied for the free surfaces between electrodes. Such boundary conditions are far more realistic than the assumption by Barnes et al. [12] of a ground plane parallel to the top surface.

The boundary conditions at an ohmic contact are that the potential is uniform and equal to the applied voltage and, in addition, that the charge density is equal to the donor value. The second assumption is an approximation that is valid within a few Debye lengths from a real ohmic contact.

A Schottky-barrier gate has different boundary conditions. Because of the difference in work functions between the metal and the semiconductor, the potential at the Schottky boundaries is less than the applied potential by ϕ_{bi}, where ϕ_{bi} is the built-in, or diffusion, potential. For convenience the voltage of the gate, V_2 in Fig. 2, will hereafter be designated as the net voltage, that is, the applied value less the built-in voltage. Thus a solution for the conditions $V_1 = V_2 = 0$ actually is the case of an applied positive bias on the gate.

The mobile charge density at the Schottky-gate electrode boundary is taken as zero, as some depletion will always occur. Since the gate boundary is always assumed to have a net reverse bias, no conduction current to it is permitted. However, displacement current will exist.

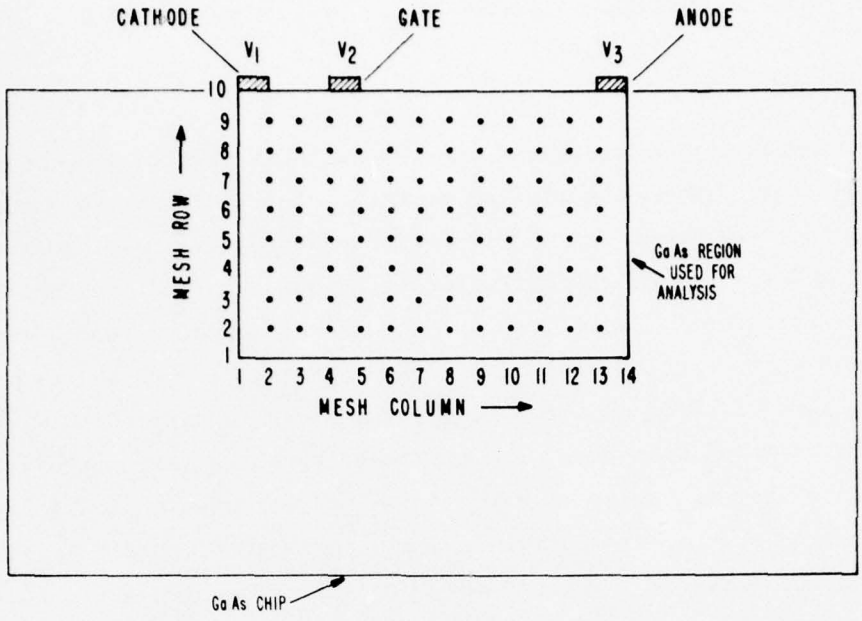


Figure 2. Cross-sectional view of planar TELD model. Mesh points are labeled as to row number and column number.

B. DERIVATION OF EQUATIONS

The fundamental variables are voltage V(I,J,t) and mobile (electron) charge density N(I,J,t), where I is the mesh column number, J is the mesh row number, and t is time.

Poisson's equation and the equation of current continuity are

$$\nabla^2 V = \frac{Q}{\varepsilon} \cdot (N_D - N) \tag{1}$$

$$Q \frac{\partial N}{\partial t} = \nabla \cdot \bar{J} \tag{2}$$

where Q = the magnitude of electronic charge

ε = the dielectric constant of GaAs

N_D = the ionized donor density

$\bar{J}$ = the conduction current

The electron conduction current consists of drift and diffusion terms:

$$\bar{J} = -QN\bar{v} + QD\nabla N \tag{3}$$

where D = the electron diffusion coefficient

$\bar{v}$ = the electronic drift velocity

Evaluation of electronic drift velocity turns out to be so complicated that a separate subroutine, called "VEL," is used in the FORTRAN program. The velocity component in any given direction is evaluated as a function of $|E|$, the *magnitude* of electric field in the region as

$$\bar{v} = \frac{\bar{E}}{|E|} \cdot |v| \tag{4}$$

where $|v| = v(|E|)$ (5)

This procedure is necessary because $v(|E|)$ is a highly nonlinear function. The relationship assumed here is of the form

$$v(|E|) = \frac{\mu|E| + v_s |E/E_c|^4}{1 + |E/E_c|^4} \tag{6}$$

where μ = electron low-field mobility

v_s = electron saturation velocity

E_c = the critical field parameter

Figure 3 shows the values of velocity as a function of electric field for various values of μ with $v_s = 0.96 \times 10^7$ cm/s and $E_c = 3.9$ kV/cm.

These values were obtained by seeking the best approximations to the velocity-field relation for 300K obtained by Bauhahn and Curtice [15] by the Monte Carlo technique. The above values of v_s and E_c were used throughout this study. The choice of the value of μ used for a particular device is based upon the donor density. Low-field mobility is known to decrease as donor

15. P. E. Bauhahn and W. R. Curtice, "Monte Carlo Calculation of the Drift Velocity of Electrons in n-GaAs," Proc. IEEE 60(9), 1106-1107 (1972).

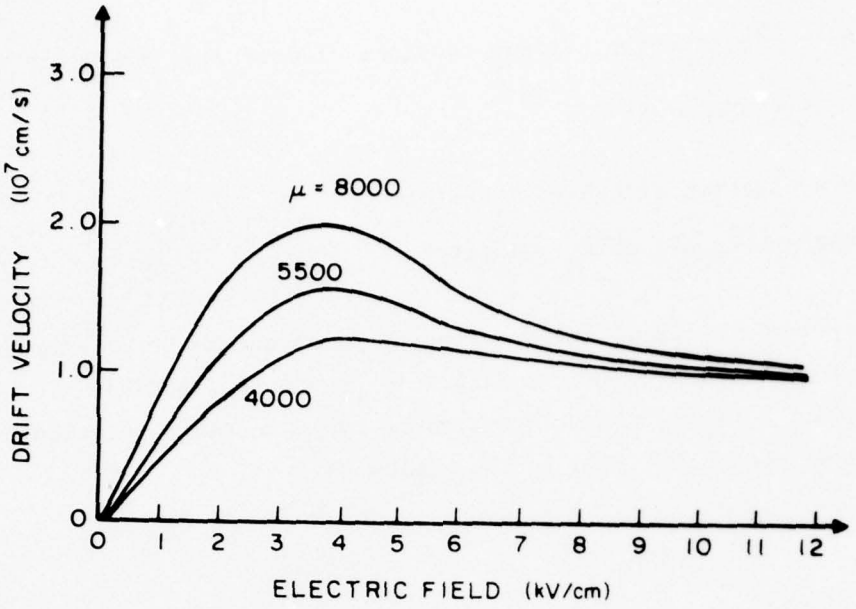


Figure 3. Calculated velocity-field relationship for Eq. (6) for three values of mobility, μ, with $v_s = 0.96 \times 10^7$ cm/s and $E_c = 3.9$ kV/cm.

density is increased; the rate of the decrease depends upon the amount of compensation. Jolly et al. [16] show that a compensation factor of 2 is realistic for good-quality material. Therefore values of $\mu = 5500$ cm^2/V-s and 8000 cm^2/V-s are used for $N_D = 10^{16}$/cm^3 and 10^{15}/cm^3, respectively, at 300K.

For example, the x component of drift velocity at a point where the components of electric field are E_x, E_y is given by

$$v_x = \frac{E_x}{\sqrt{E_x^2 + E_y^2}} \cdot v\left(\sqrt{E_x^2 + E_y^2}\right) \tag{7}$$

The relationship shown in Eq. (6) must be used to evaluate the magnitude of drift velocity.

16. S. T. Jolly, L. C. Upadhyayula, H. C. Huang, and B. J. Levin, "Junction Growth Techniques for GaAs Avalanche Transit-Time Devices," U.S. Army Electronic Command, Fort Monmouth, N. J., ECOM-0308-F, 1973.

The diffusion coefficient D will be taken as constant and equal to $(kT/Q)\mu$ for most calculations. The effects of assuming a field-dependent diffusion coefficient, as Yamaguchi et al. [9] have done, appear to be minor. This is investigated further in Section III.

Poisson's equation and the continuity equation are written as difference equations for use with the array of points. Figure 4 shows a group of nine points anywhere inside the device. When the notation of this figure is used,

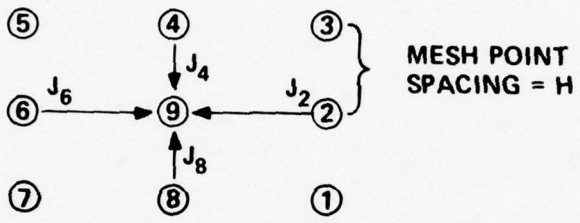


Figure 4. Point array inside the device. The subscripted J's designate *electron* conduction currents.

Poisson's equation becomes:

$$V_9 = \frac{V_2 + V_4 + V_6 + V_8}{4} - \frac{QH^2}{4\varepsilon}(N_9 - N_D) \tag{8}$$

where the subscript denotes the point number. The value of the divergence of current at point no. 9 can be evaluated by use of the divergence theorem on the volume integral of $\nabla\cdot\bar{J}$ around point no. 9. The divergence theorem is

$$\int_{\substack{\text{Volume}\\ \nu}} \nabla \cdot \bar{J} d\nu = \oint_{\substack{\text{Surface}\\ \text{of } \nu}} \bar{J} \cdot \overline{dS} \tag{9}$$

where v is the volume whose center is the mesh point and whose sides are H by H by unity width. Replacing $\nabla\cdot\bar{J}$ by $Q\,\partial N/\partial t$ and approximating both integrations gives, for Eq. (9),

$$Q\frac{\partial N}{\partial t}H^2 = (J_2 + J_4 + J_6 + J_8)H \tag{10}$$

or

$$\frac{\partial N}{\partial t} = \frac{J_2 + J_4 + J_6 + J_8}{QH} \tag{11}$$

where J_2 is the amount of *electron* current flow. The change in N for each time step is evaluated in this study by explicit means as

$$\Delta N = \frac{J_2 + J_4 + J_6 + J_8}{QH} \cdot \Delta t \tag{12}$$

as opposed to using the more sophisticated implicit techniques discussed by Reiser [6].

An inherent advantage of the mathematical form of Eq. (12) is that large changes in charge density can be accommodated by using small time steps. Generally, as the donor density is increased, the time step must be decreased proportionally. The time step is usually taken to be about the value of dielectric relaxation time, $\varepsilon/N_D e\mu$, for the device under study. If the total computed currents across two parallel planes between electrodes are not equal, the time step is reduced. Reiser [17] shows that if the time step is

$$\Delta t \leq \text{MIN} \left\{ \frac{H^2}{4D}, \frac{2D}{v^2} \right\} \tag{13}$$

then the solutions of the difference equations are (conditionally) stable. Thus the time step will be less than the dielectric relaxation time if the mesh spacing is very small.

To describe the depletion region accurately, the mesh spacing, H, should be chosen to be of the order of the intrinsic Debye length [18] given by $\sqrt{kT\varepsilon/Q^2N_D}$. This, however, leads to very small values for H(0.06 μm for kT/Q = 0.05 V and $N_D = 10^{16}/cm^3$) and an excessive number of mesh points. Larger values of H have therefore been used in this study, resulting in a loss of accuracy in the definition of the depletion region.

The value for each current component in Eq. (12) must be evaluated by Eq. (3), for example,

$$J_6 = Q \frac{N_6 + N_9}{2} \cdot v_{96} - \frac{DQ}{H}(N_9 - N_6) \tag{14}$$

17. M. Reiser, "Large-Scale Numerical Simulation in Semiconductor Device Modelling," Computer Methods in Appl. Mech. Eng. 1, 17-38 (April 1972).
18. J. P. McKelvey, *Solid State and Semiconductor Physics* (Harper & Row, New York, 1966), pp. 332-333.

where v_{96} is the velocity component from point no. 6 to point no. 9. The magnitude of the electric field for evaluation of v_{96} is taken as E_{96} where

$$E_{96} = \frac{1}{H}\left\{(V_9 - V_6)^2 + \frac{1}{16}(V_4 - V_8 + V_5 - V_7)^2\right\}^{1/2} \tag{15}$$

The velocity component v_{96} is then

$$v_{96} = \frac{V_9 - V_6}{H\,E_{96}} \cdot v(E_{96}) \tag{16}$$

The simulation program consists of first applying Poisson's equation [Eq. (8)] point by point, row by row, until the largest change in voltage from one iteration to another is less than a specified value (usually 0.0001 v). A potential solution is then available. One time step is taken by applying Eq. (12) once to each point. Poisson's equation is then solved again for the new voltage array at the new time. The process continues and a transient solution is obtained.

Figure 5 shows a more detailed flow chart for the solution of the model depicted in Fig. 2. Note that the program is written to include the semi-insulating substrate. Initialization of the problem can be done arbitrarily or can be read from a file containing a previous solution. A nonphysical initialization automatically relaxes to a real solution after sufficient time steps.

Poisson's equation (in difference form) is solved by successive overrelaxation with a relaxation factor determined by the number of mesh points. For example, each internal point, such as no. 9, has the following routine applied at each iteration:

$$V_9^{OLD} = V_9 \tag{17}$$

$$V_9^{NEW} = \frac{V_2 + V_4 + V_6 + V_8}{4} - \frac{QH^2}{4E}(N_9 - N_D) \tag{18}$$

$$V_9^{NEW} = V_9^{NEW} + F \cdot (V_9^{NEW} - V_9^{OLD}) \tag{19}$$

where F is the acceleration factor, whose value lies between 0 and 1. The acceleration factor is chosen to accelerate convergence by reducing the number of iterations. The reduction of the number of iterations more than compensates for the increased number of computations required at each point by the above set of equations. The conventional overrelaxation factor as described by Hockney [19] is equal to (1 + F).

As noted in Fig. 5, the first and last rows are treated separately because of the boundary conditons. The same holds true when N is updated for the time step.

Figure 5 shows that the total current at each electrode can be evaluated and that N and V array values can be saved when desired. Some of these data are usually printed out at every tenth time step to check that no numerical problems exist. The total current is calculated as the sum of electron conduction current and displacement current across a plane through the device. The inspection of total current values has proven to be the best method of checking the accuracy of a solution.

19. R. W. Hockney, "The Potential Calculation and Some Applications," Methods in Computational Physics 9, 135-211 (1970).

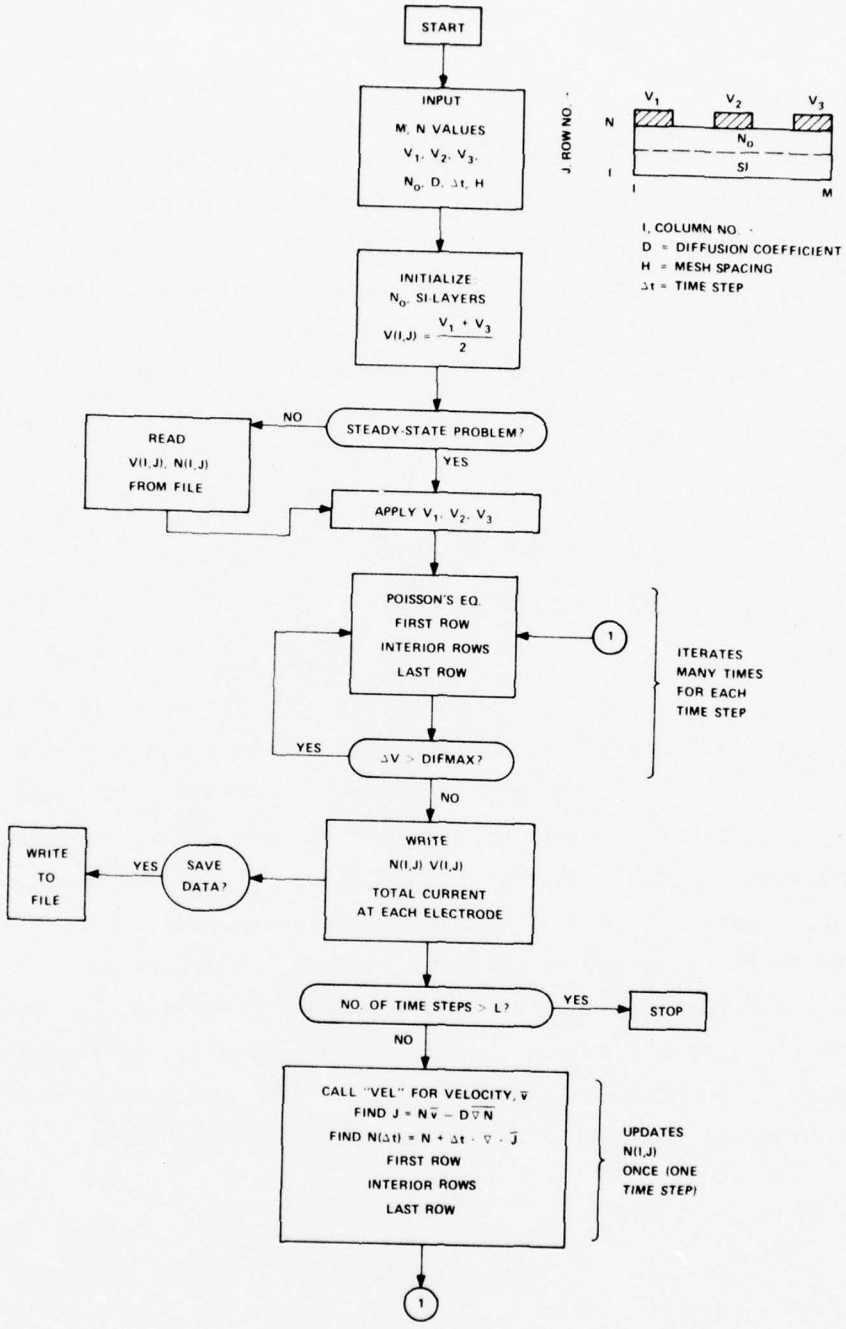


Figure 5. Program flow and device model for the transient analysis.

III. COMPUTER SIMULATION OF PLANAR TE DIODES

A. A 5-μm DEVICE

The planar TE diode was simulated principally to study the behavior of the computational program. A relatively short diode (5 μm) was used for the convenience of short execution time. Although it is well known that such devices deviate from transit-time behavior because of the time required for intervalley transfer, this effect is neglected in our study.

Figure 6 shows the structure of the TE diode. Note that the contact regions and the semi-insulating substrate are included in the simulation. At time t = 0,

$$N(I, J) = \begin{cases} N_D & \text{in the N layer} \\ N & \text{in the SI layer} \end{cases} \tag{20}$$

and the anode voltage is applied instantaneously. The solution of Poisson's equation at t = 0 is actually a solution for Laplace's equation, as the space charge is zero. Because of the planar contacts, the electric field is significantly larger at the (interior) edge of the cathode electrode than in the N layer. As time steps are taken, charge depletion develops naturally at the cathode edge, together with some charge accumulation, and a high field domain grows easily from the region beneath the cathode. Thus, no artificial doping notch is required in this model to produce domain formation. As Suzuki et al. [7] point out, this results from the field distortion in the vicinity of the planar cathode, a natural consequence of the two-dimensional geometry.

For the initial case, the following parameters were used:

$$\begin{aligned} &\text{Cathode} = 0\ \text{V} \\ &\text{Anode} = 3\ \text{V} \\ &N_D = 2 \times 10^{15}/\mu\text{m}^3 \\ &\mu = 8000\ \text{cm}^2/\text{V-s} \\ &D = 200\ \text{cm}^2/\text{s} \\ &H = 0.25\ \mu\text{m} \\ &\Delta t = 0.2\ \text{ps} \end{aligned} \tag{21}$$

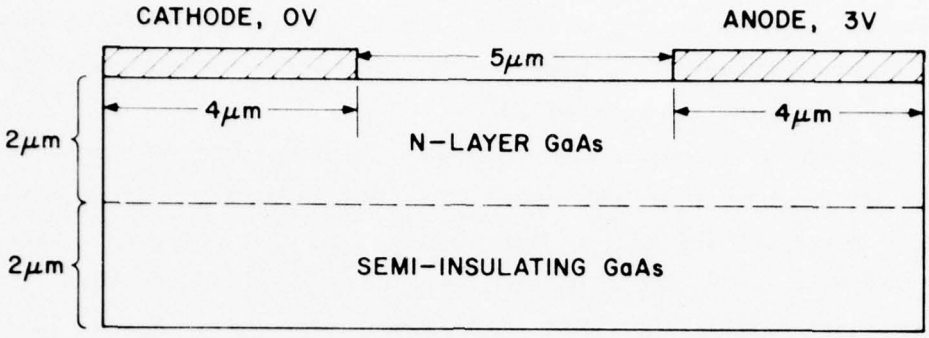


Figure 6. A two-terminal, planar TELD.

Figure 7 shows the potential and electric fields along the surface of the device as a function of the distance from the cathode at two values of time. At 20 and at 45 ps a distinct high-field domain is present. Inspection

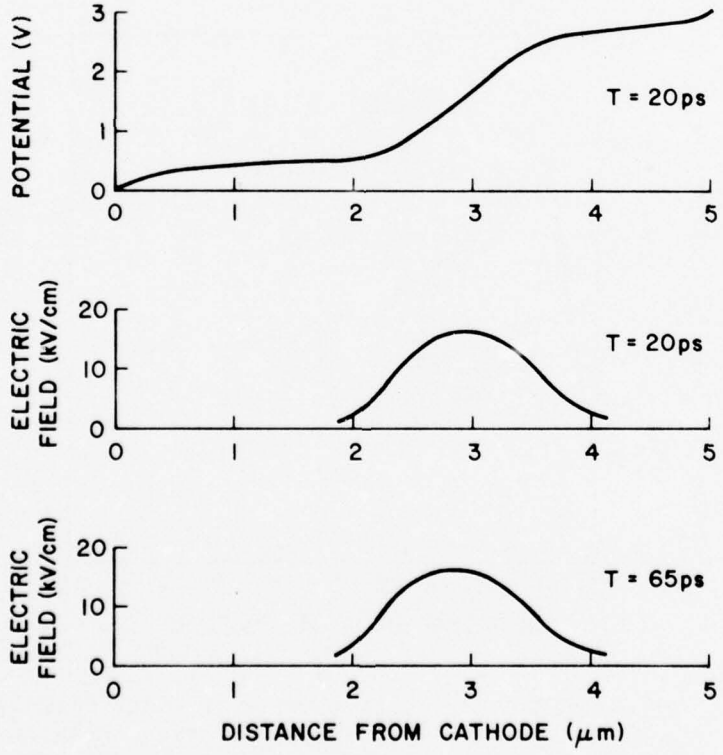


Figure 7. Potential and electric fields as a function of distance from the cathode for the device of Fig. 6.

of the charge density array shows that there is an accumulation layer preceded by a depletion layer. The reoccurrence of the same position of the domain at 65 ps indicates a transit-time period of 45 ps. This is consistent with an expected transit-time frequency of 20 GHz.

Figure 8 shows the calculated values of total current (per unit width) as a function of the number of time steps for the same device. Three different planes have been used for this calculation. As no displacement or diffusion current exists at t = 0, the situation is nonphysical, and the total current values are quite different at different planes. After only a few time steps, however, the currents are seen to converge to the same value within a small error. After 10 time steps (t = 2 ps), the current evaluated at a cathode or anode plane differs by less than 1% from that evaluated 1 μm from the cathode. This demonstrates that if H and Δt are chosen for numerical stability, the model relaxes rapidly from a nonphysical set of initial conditions to an accurate physical transient solution.

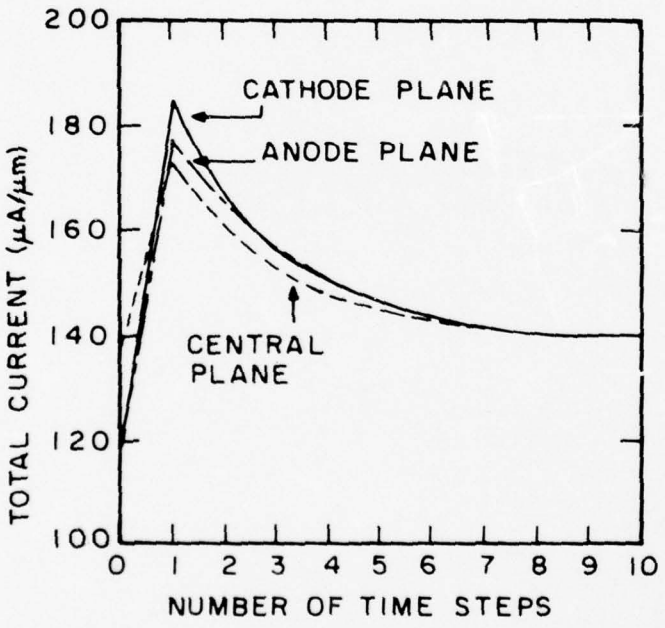


Figure 8. Calculated total current per unit width flowing across several planes vs the number of time steps for the TE diode of Fig. 6. Cathode plane is 0.125 μm from cathode; anode plane is 0.125 μm in front of anode; central plane is 1.0 μm from cathode.

Figure 9 shows the total current through this device as a function of time. The total number of time steps used is 100 ps/0.2 ps = 500. Poisson's (difference) equation is iterated an average of 50 times each time step to reduce DIFMAX (the maximum voltage change between iterations) to less than 0.0001 V. If any numerical instabilities or computational accumulating inaccuracies were present, the regular transit-time oscillations would not be produced. Clearly the results are not very dependent upon the initial conditions in time.

Note that the current drop, $\Delta I/I$, defined as

$$\frac{I_{max} - I_{min}}{I_{max}}$$

is 32% for Fig. 9. This has been produced by a bias slighly above threshold and a v-E relationship with a peak/valley (P/V) ratio of 2.06. A larger current drop can be obtained by anode-biasing a device of larger doping-length ($n\ell$) product to several times the threshold value. The problem in this device of relatively low $n\ell$ product ($\tilde{\sim}10^{12}/cm^2$) is that the domain size (see Fig. 7) is an appreciable fraction of the anode-cathode spacing.

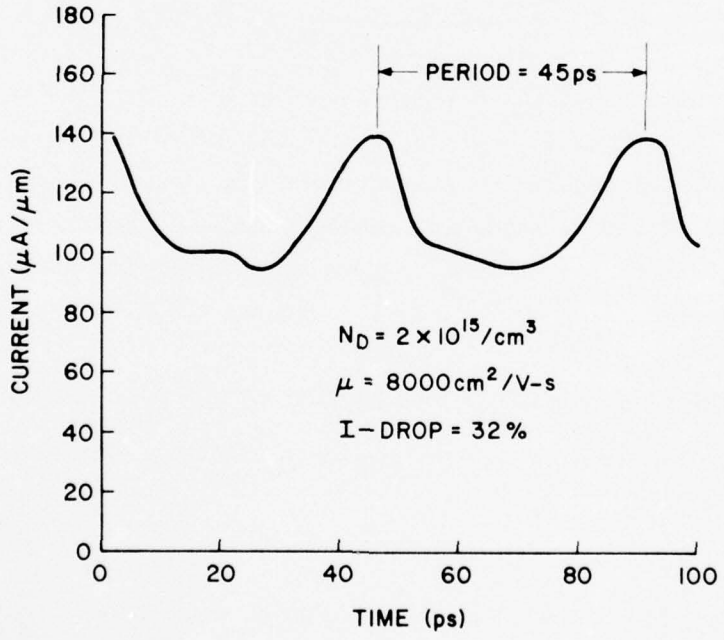


Figure 9. Current per unit width vs time for two-terminal planar TED with an anode voltage of 3 V.

Figure 10 shows the total current as a function of time for increased doping ($N_D = 5 \times 10^{15}/cm^3$). The current waveforms are slightly changed because the domain is smaller. The current drop at 3 V is 34% and, at 6 V, increases to 37%.

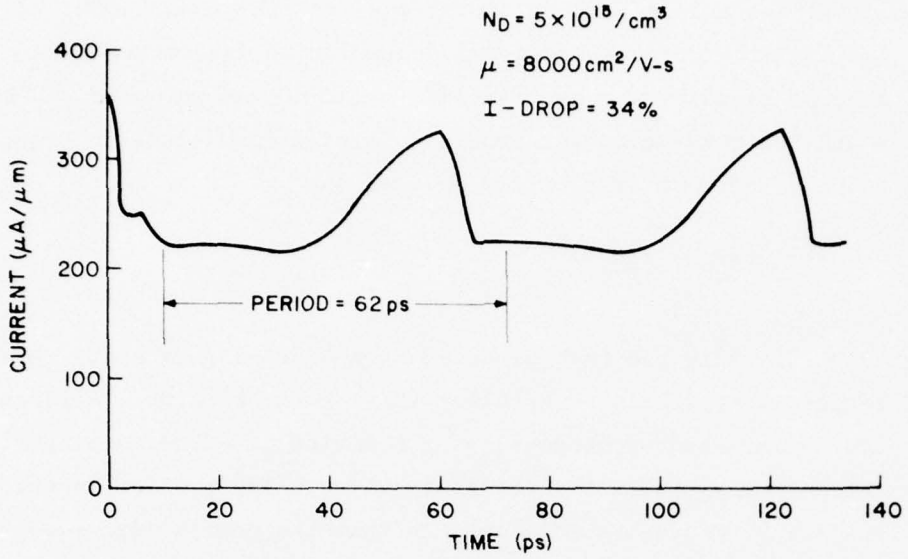


Figure 10. Current per unit width vs time for a planar TED diode with increased N_D and an anode voltage of 3 V.

Figure 11 shows the total current as a function of time for a case similar to that shown in Fig. 10, but where $\mu = 5000\ cm^2/V\text{-}s$. This causes the P/V ratio to be about 1.4 and reduces the current drop to only 17% at 3 V. A comparison of Figs. 10 and 11 shows the valley current to be about the same and the principal change to be a reduction in peak (and threshold) current. If the anode voltage is increased to 5 V, $\Delta I/I$ increases to 21.5%.

B. EFFECT OF THE FIELD DEPENDENCE OF DIFFUSION

In the single-carrier model assumed for GaAs, the diffusion current has been taken as

$$QD\nabla N \tag{22}$$

This is the simplified form of the more general expression

$$Q\nabla(DN) \tag{23}$$

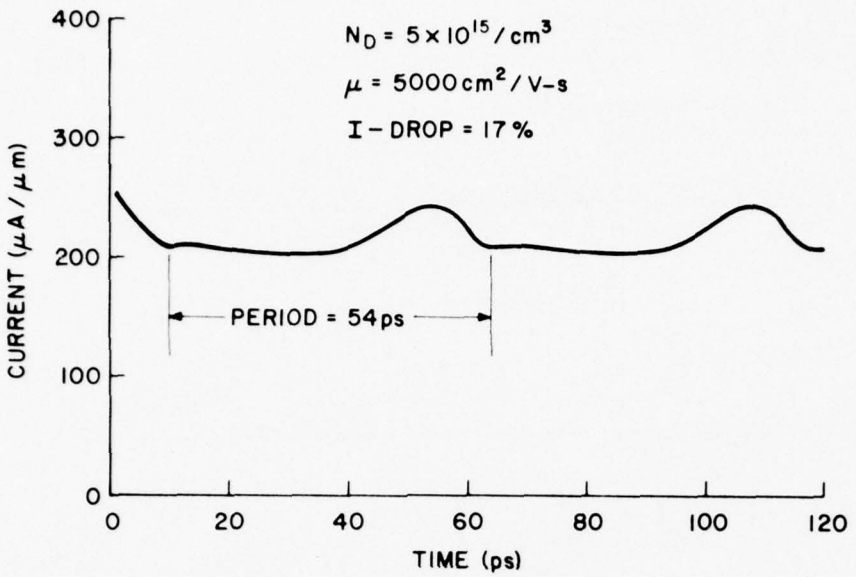


Figure 11. Current per unit width vs time for a planar TED diode with reduced mobility and for an anode voltage of 3 V.

Thus, if the diffusion coefficient is taken to be field dependent, an extra term is added to QDVN to account for the gradients in the electric field. This extra term is of thermoelectric origin and represents current caused by (carrier) temperature gradients. However, it is questionable whether the inclusion of this term is worthwhile, since its accurate evaluation depends upon the details of electron heating as calculated by the Boltzmann transport equation [20]. Because this analysis has assumed a single-carrier model with drift and diffusion properties dependent upon the local average value of electric field, omission of the thermoelectric term is appropriate. In this section the diffusion current will be evaluated by use of the expression QDVN. The only effect of the field dependence will be to change the magnitude of the diffusion coefficient.

20. K. Blotekjaer, "Transport Equation for Electrons in Two-Valley Semiconductors," IEEE Trans. Electron Devices ED-17(1), 38-47 (1970).

Figure 12 shows the assumed form of the diffusion coefficient. This curve is approximately the same as that calculated by Butcher et al. [21], and is only slightly different from that derived by Fawcett and Rees [22]. The analytical expression assumed is

$$D = 180 + \frac{200}{1 + 10(1 - \frac{E}{3.5})^2} - 4E \text{ cm}^2/\text{s} \qquad (24)$$

where E is the electric field in kV/cm.

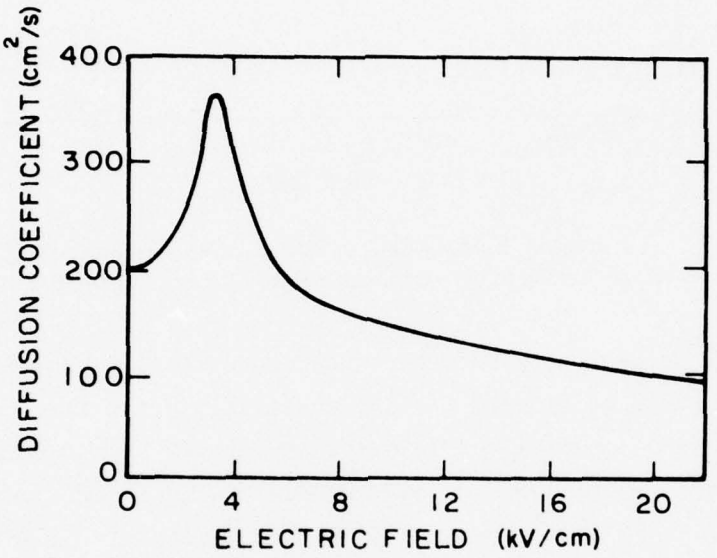


Figure 12. Diffusion coefficient as a function of electric field.

The subroutine VEL was modified in such a way that each time the magnitude of electric field was evaluated in a region of six points to evaluate a velocity component, the value of diffusion was found, too. Thus in any group of nine points (as in Fig. 4), four diffusion values are found for diffusion to or from the center point.

21. P. M. Butcher, W. Fawcett, and W. R. Ogg, "Effect of Field Dependent Diffusions in Stable Domain Propagation in the Gunn Effect," Brit. J. Appl. Phys. 18, 755-759 (June 1967).
22. W. Fawcett and H. D. Rees, "Calculation of the Hot Electron Diffusion Rate for GaAs," Phys. Lett. 29A, 578-579 (Aug. 1969).

A simulation of the 5-μm TE diode with $N_D = 5 \times 10^{15}/cm^3$ was made with D(E) of Eq. (24). The results were only slightly different from the previous simulation with constant D. Figure 13 shows the charge density at the surface for the two cases at t = 20 ps. Clearly, no appreciable difference is present. This means that diffusion effects are of relatively minor importance. Because of this, no further simulations were made with a field-dependent diffusion coefficient.

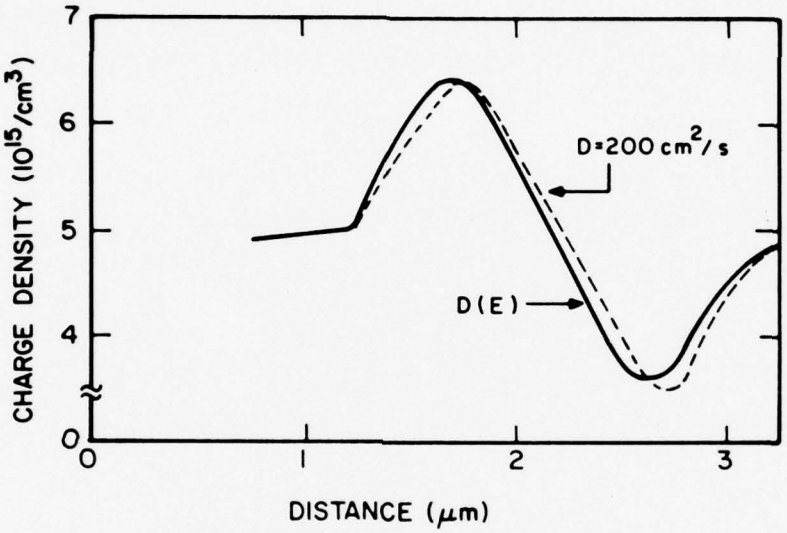


Figure 13. Charge density at the surface as a function of position for the TED diode of Fig. 6 with $N_D = 5 \times 10^{15}/cm^3$ and t = 20 ps.

C. WIDTH TAPERING

The effects of a gradual taper in the TE device's width can be approximated without resort to an extremely complex, three-dimensional model. It is assumed that the principal effect is upon charge (and current) density and not upon solution to Poisson's (difference) equation. Current flow in the transverse direction is neglected. The current continuity [Eq. (10)] will be rederived with a gradual taper of the width.

The width ratio in one mesh spacing, H, is assumed to be $(1 - (\Delta/2)]/[1 + (\Delta/2)]$, where Δ is a small number (positive or negative). For a tapered section containing m mesh points the width ratio is

$$\left(\frac{1 - \frac{\Delta}{2}}{1 + \frac{\Delta}{2}}\right)^m \tag{25}$$

Figure 14 shows the top and side view of a typical (interior) volume element for which the divergence theorem [Eq. (9)] will be applied. A point array similar to the one in Fig. 4 is also shown. Since the volume of this tetrahedron is now $H^2 \cdot H'$, the volume integral of $D \cdot \bar{J}$, or $Q\frac{\partial N}{\partial t}$, is

$$Q \frac{\partial N}{\partial t} \cdot H^2 \cdot H' \tag{26}$$

and the (complete) surface integral of $\bar{J} \cdot \bar{dS}$ then is

$$J_2 \cdot H \cdot H' \cdot (1 - \frac{\Delta}{2}) + J_4 \cdot H \cdot H' + J_6 \cdot H \cdot H' \cdot (1 + \frac{\Delta}{2}) + J_8 \cdot H \cdot H' \tag{27}$$

Equating these expressions,

$$\frac{\partial N}{\partial t} = \frac{J_4 + J_8 + J_2(1 - \Delta/2) + J_6(1 + \Delta/2)}{QH} \tag{28}$$

This equation replaces Eq. (11) and causes the tapering to affect the change in the charge-density array, N(I,J), each time step. If the simulation is performed accurately, the device's total current density should increase in regions of narrower width, so that the total current flow across any two (transverse) planes between electrodes is still the same.

The TE diode of Fig. (6) was used as a test structure. Two cases were simulated. Case no. 1 is for a width reduction going from cathode to anode.

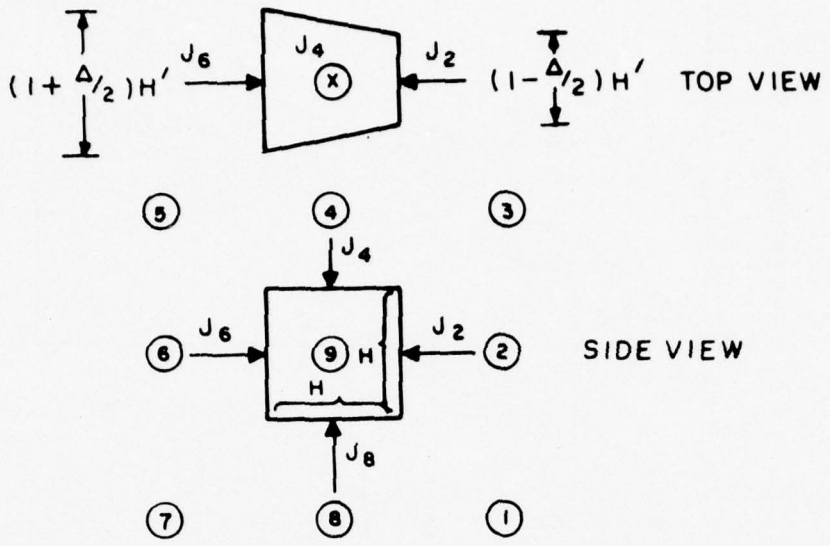


Figure 14. A volume element in the point array of tapered-width device.

Case no. 2 is for a width expansion, going from cathode to anode. In both cases it was assumed that

$$
\begin{aligned}
|\Delta| &= 0.0091 \\
m &= 18 \\
\left(\frac{1 - \Delta/2}{1 + \Delta/2}\right)^m &= 0.85 \\
\mu &= 5000\ \text{cm}^2/\text{V-s} \\
N_D &= 5 \times 10^{15}/\text{cm}^3 \\
\text{Anode voltage} &= 3\ \text{V}
\end{aligned}
\tag{29}
$$

For case no. 1, the tapering-in causes the largest electric fields to occur near the anode, leading to a stable condition with no transit-time oscillation. Very large charge accumulation occurs at the anode and produces a large anode drop (in voltage). Figure 15 shows the computed surface potential as a function of distance from the cathode for case no. 1 and the case without taper. At $t = 0$, the potential profiles are the same. At $t = 20$ ps, an anode drop occurs in case no. 1, but a traveling high-field domain is present for the case without taper.

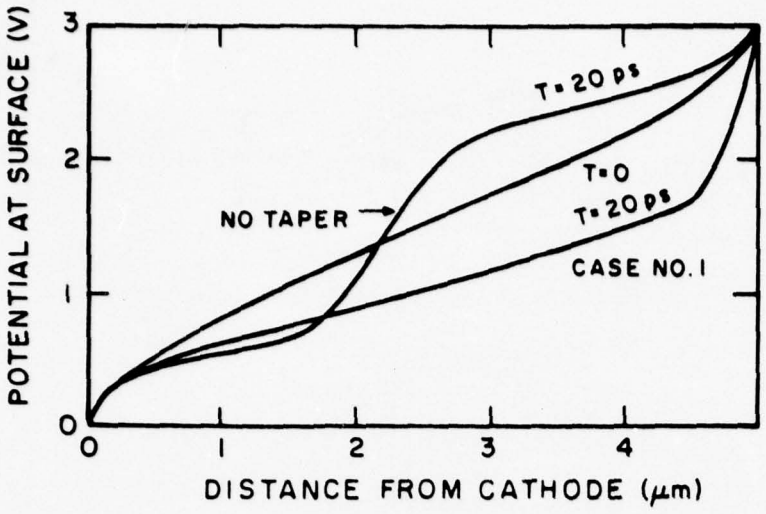


Figure 15. Surface potential as a function of distance from the cathode for a tapered TED diode (case no. 1) and a nontapered TED diode.

Figure 16 shows the current waveform (at the cathode) for case no. 2. In this instance the narrow width at the cathode favors domain formation in that region and results in transit-time oscillation. Notice, however, that the shape of the current waveform is influenced by, and in fact reflects, the shape of the device. This can be seen by comparison with Fig. 11.

For the simulation of Fig. 16, the total current flow at the anode is typically between 1 and 2% larger than the cathode current. In the case without taper, these currents agree within $\pm$ 0.5%. Some increased inaccuracy has resulted, but is not important.

D. MODELING OF THE OHMIC CONTACT REGIONS

In most planar TE devices, the anode and cathode contact regions are purposely made about twice the width of the active device. This is done to reduce the resistance of these regions by providing large contacting areas. One technique of accounting for this is to simulate larger doping beneath the ohmic contacts. The contacting regions thus exert less influence upon the device's behavior. This procedure also permits simulation with much shorter contact lengths, and is desirable because it reduces the number of mesh points and thus the computational time.

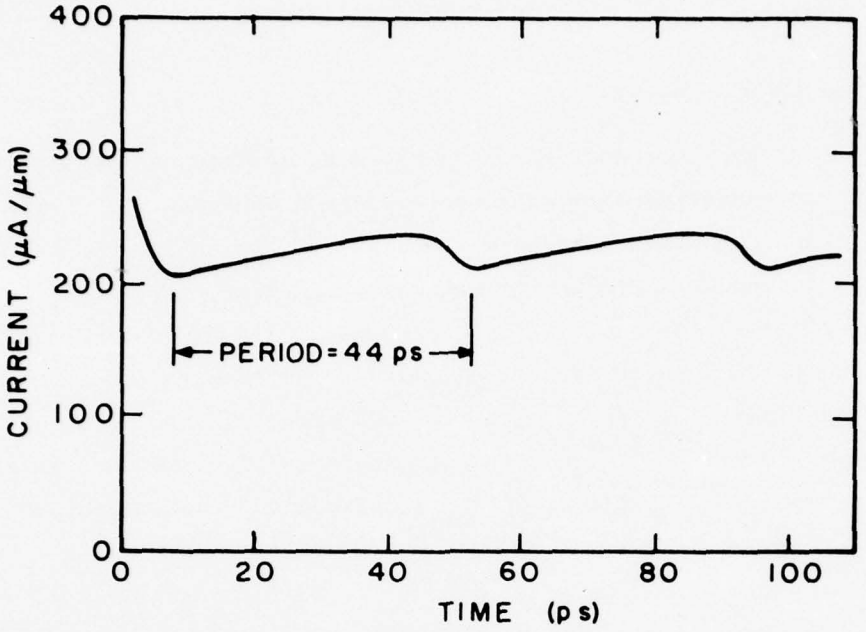


Figure 16. Current as a function of time for the tapered TED diode (case no. 2).

Goto et al. [8] and others have used an ionized carrier density of five times the numerical doping value at the ohmic contacts. Between the electrode and the active region, a buffer region is set up where the domain density changes gently over a few microns. This is a more complicated procedure and is probably unnecessary in most device simulations.

Several device simulations in which carrier density N_D was assumed at the contacts and below produced nonphysical results that disappeared when a $2N_D$ doping was used under the contacts. In particular, a larger anode drop (in voltage) sometimes would occur for N_D contact doping but disappear for $2N_D$ contact doping. Likewise, some voltage instabilities under the cathode contact were suppressed by $2N_D$ doping under the cathode.

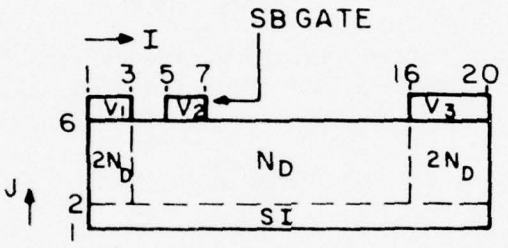
For the remainder of this report, $2N_D$ doping under the ohmic contacts will generally be assumed.

IV. THREE-TERMINAL TELDs

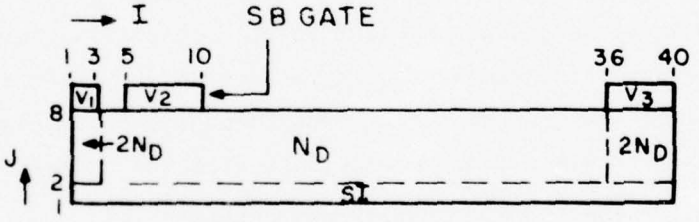
A. BASIC DEVICE PROPERTIES

Both the enhancement and depletion types of devices can be simulated. This section is concerned only with the depletion devices. Some preliminary results for the enhancement mode are given in the Appendix.

Two device models were studied extensively. Figure 17 shows the dimensions and doping of these two models. For these studies, μ was taken to be 5500 $cm^2/V\text{-}s$. The dimensions of these models are very close to two types of experimental devices fabricated in a concurrent ONR program. The major difference is that the experimental devices use thinner and more highly doped epitaxial layers. However, the "nd" product (i.e., doping density times epitaxial layer thickness) is about the same, viz. 3-4 x $10^{12}/cm^2$.



(a)



(b)

Figure 17. (a) A 13-μm TELD model; $N_D = 1 \times 10^{16}/cm^3$. Each division is one micron.
(b) A 33-μm TELD model; $N_D = 5 \times 10^{15}/cm^3$. Each division is one micron.

Figures 18 and 19 show the I-V (current-voltage) relationships computed for these two devices. Each device exhibits an ohmic I-V region, a current saturation region near threshold, and a transit-time region above threshold voltage. The peak and valley currents for the domain-mode transit-time region are shown. Neither device exhibits a domain-sustaining voltage less than threshold, such as is common to sandwich-type TEDs. In fact, each device must be biased about 10% above threshold voltage before proper transit-time behavior is present. Figure 20 shows proper transit-time behavior occurring at 5-V bias, but not at 4.2-V bias on the 13-μm device. At 4.2 V the domain disappears before reaching the anode, and a new domain forms immediately. In either device, if a domain is formed by anode bias well above threshold, it will disperse if the anode bias is reduced to threshold value.

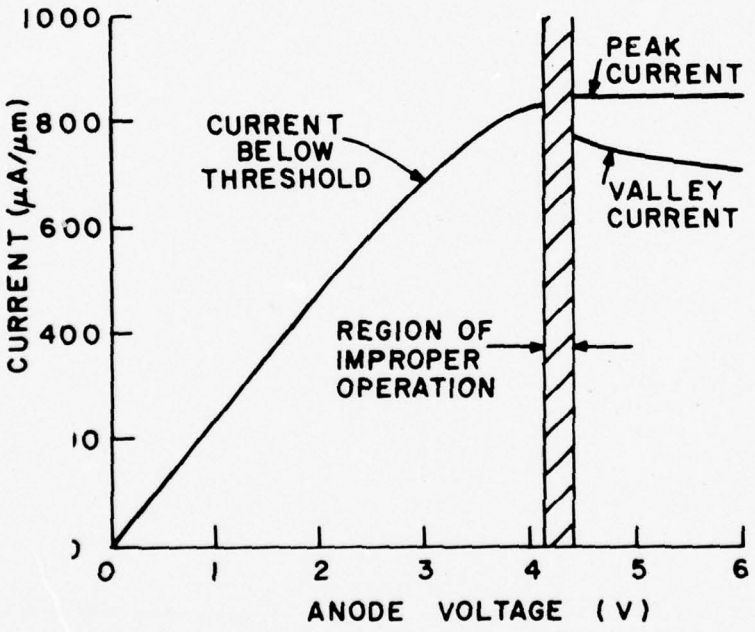


Figure 18. Anode current as a function of anode voltage for the 13-μm TELD of Fig. 17(a) with $V_2 = 0$.

A reduction in both the current drop above threshold and the anode-threshold-voltage value is observed when the gate is biased more negatively in experimental devices. These effects are also observed in the device simulations.

The dipole domain forms at the anode edge of the Schottky-barrier gate. The development of the accumulation and depletion regions of the domain is

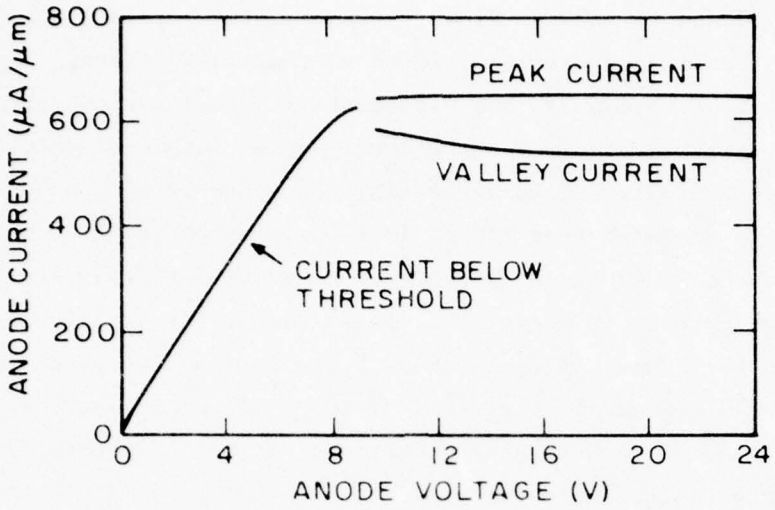


Figure 19. Anode current as a function of anode voltage for the 33-μm TELD of Fig. 17(b) with $V_2 = 0$.

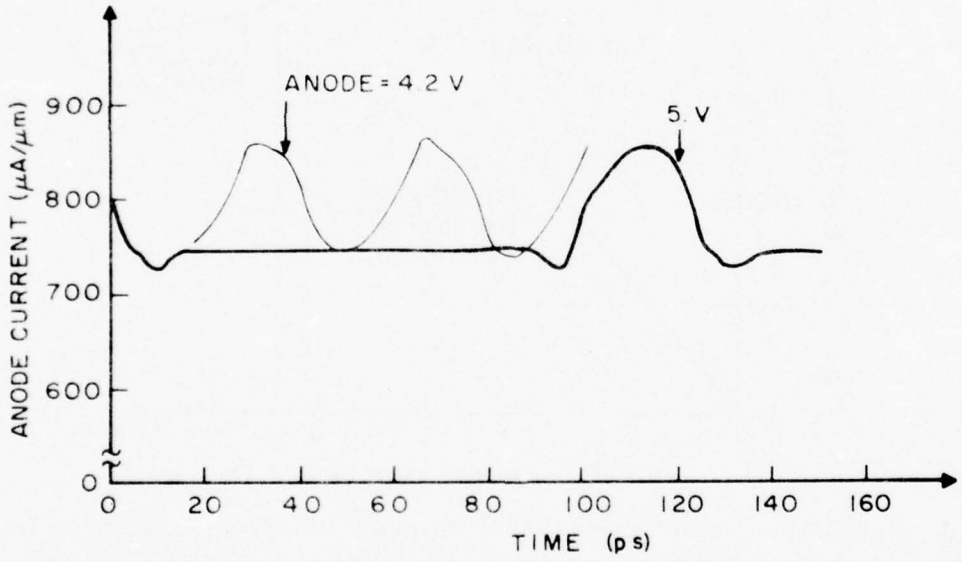


Figure 20. Anode current as a function of time for the 13-μm TELD of Fig. 17(a) with $V_2 = 0$.

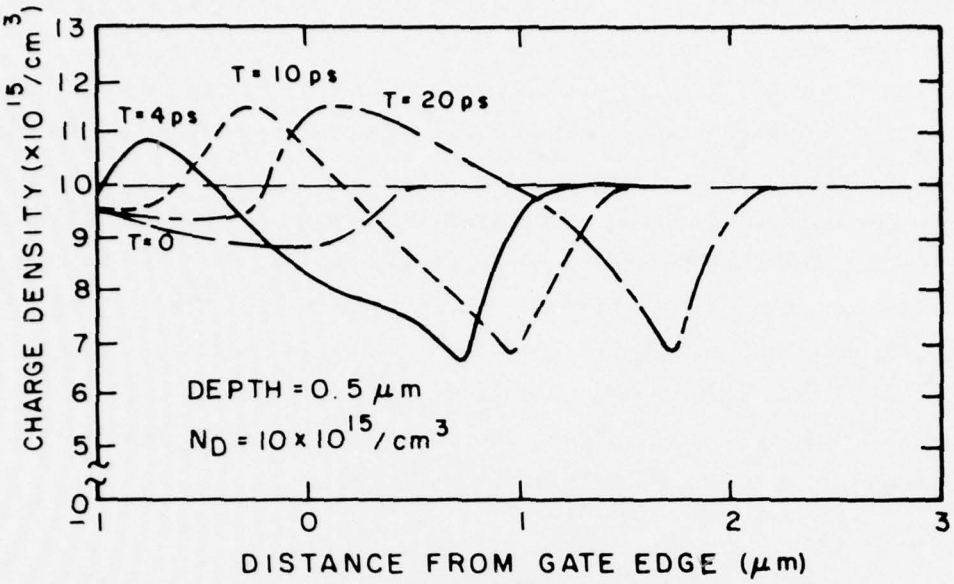


Figure 21. Charge density as a function of position at 0.5 μm below the gate for the 13-μm TELD with V_3 = 4 V at $t < 0$ and V_3 = 6 V at $t \geq 0$.

illustrated in Fig. 21. Here the charge density is plotted as a function of distance from the gate's edge at 0.5 μm beneath the gate. The anode bias is changed from 4 to 6 V at T = 0, and domain growth occurs. After the charge accumulation and depletion regions develop, a drift toward the anode is present. It is not until t = 23 ps that the accumulation layer hits the surface of the device. Shortly after this, at t = 28 ps, a stable domain is present and the anode and cathode currents are constant until the domain reaches the anode.

Table 1 presents a summary of the properties of the two device models. Notice particularly that both devices have about the same peak-to-valley current

TABLE 1. DEVICE PROPERTIES

Device Length (μm)	Donor Density, N_D (10^{15}/cm^3)	Epi-Thickness (μm)	Threshold Voltage, V_{TH} (V)	Assumed Width (μm)	Threshold Current, I_{TH} (mA)	Low-Field Resistance (Ω)	Transconductance g_m (mV)	TT* Period at 1.5 V_{TH} (ps)	P/V Current Ratio at 1.5 V_{TH}	Series Resistor, R_{gate} (Ω)	Series Capacitor, C_{gate} (pF)
13	10.0	4	4.05	100	84	41	1.8	114	1.19	29	0.03
33	5.0	6	9.0	50	31	260	1.6	328	1.19	50	0.05

*Transit-time.

ratio and low values of g_m. Transit-time period corresponds to the section of the device between the gate and anode, not the cathode and anode. The equivalent circuit for the gate in each case is a series resistor and capacitor, R_{gate} and C_{gate}, respectively. These were computed from the pulse response of the gate current below threshold.

That percentage of current drop available from a three-terminal device is less than that for the equivalent two-terminal device and quite dependent upon the epi-layer thickness, d. For example, the 13-μm TELD has a 16.1% current drop at 6 V, as shown in Fig. 18. If the d value is reduced, less current drop occurs. Table 2 shows the calculated value of current drop for several changes of parameters. This effect should be studied for larger values of N_D, such as those used in the experimental devices.

TABLE 2. CALCULATED CURRENT DROP FOR THE 13-μm DEVICE AT V_3 = 6 V WITH SEVERAL PARAMETER CHANGES

Case	Gate Length (μm)	N_D ($10^{15}/cm^3$)	Epi-Thickness (μm)	$\frac{I_{max}-I_{min}}{I_{max}}$
1*	2	10	4	16.1
2	2	10	2	5.2
3	2	5	4	15.0
4	4	10	4	13.7

*Same as Fig. 17(a).

B. SWITCHING PROPERTIES OF THE DEVICE

In this section, the behavior of an individual device will be described for the case of a sudden change in anode or gate voltage. Only the short device (13 μm) has been investigated.

In one case studied for a device biased below threshold voltage, the anode voltage is suddenly switched to above threshold value. The original bias value is 4 V. Figure 22 shows the current waveforms for application of an additional 2-V anode pulse. The sudden increase in anode current is the result of displacement current, whereas the eventual current drop is the result of domain formation. For this case, a mature domain forms in about 28 ps.

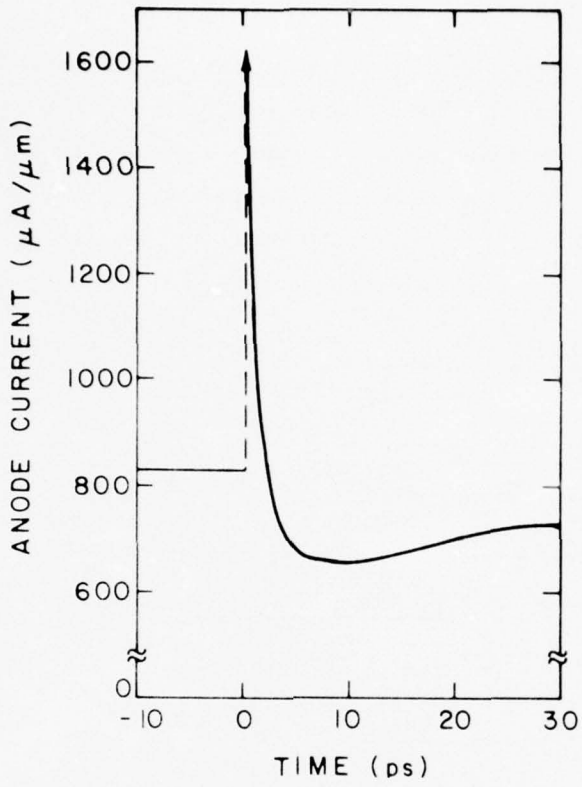


Figure 22. Anode current as a function of time for the 13-μm device with $V_1 = V_2 = 0$ V, $V_3 = 4$ V, and an anode pulse of +2 V applied at t = 0.

In another instance, an anode increase of 1 V is used. A stable domain again forms, and the formation time is nearly the same (about 26 ps). The minimum-anode-pulse voltage for stable domain mode is slightly less than 0.5 V, as seen in Fig. 18.

However, a negative pulsing of the cathode with 4 V on the anode does not cause domain formation in the 13-μm device. This behavior is a result of the particular geometry and device parameters, and is not universal. For example, Goto et al. [8] have shown that proper gate triggering of domains may occur in larger devices. In his examples he describes a device with a gate-to-anode separation of about 24 μm. The additional device length has an effect much like the adding of resistance in series with the anode of a short device.

C. SWITCHING TELDs WITH ANODE OR CATHODE RESISTANCE

The program for device simulation was modified to include either an anode or cathode resistor. In the circuit shown in Fig. 23, the short device is assumed to be biased below threshold. A negative pulse is applied to the gate, and the transient behavior is evaluated, including the effects of anode (or cathode) voltage change due to the anode resistor, R_A (or cathode resistor, R_C).

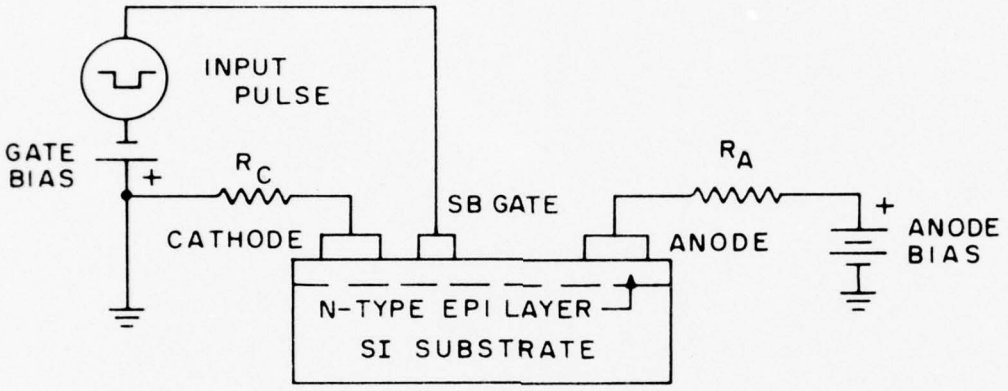


Figure 23. Circuit model assumed for gate-triggered TELD.

The amount of voltage change produced in these resistors depends upon the total current through the device. If ΔI is the current change per unit device width and W is the device width, then the voltage change produced at the anode or cathode is ΔIWR_A or ΔIWR_C, respectively. Calculations were made for various values of WR_A and WR_C, based on the assumption of a time constant of 1-2 ps for this external circuit.

Figure 24 shows the calculated anode voltage as a function of time for the 13-μm device. The device is initially biased at 4 V and has a WR_A value of 5000 Ω-μm. For a 100-μm wide device, R_A = 50 Ω; according to Table 1, this is about equal to the device's low-field resistance. The negative gate step is applied at 10 ps. For a gate step (V_G) of 0.5 V (the dashed curve) no domain results, and the anode voltage increase ($g_m R_A V_G$) is small. However, it is seen that the application of -0.7 or -0.9 V causes an increase in anode voltage due to a sudden decrease in anode current. The current decrease is due to domain

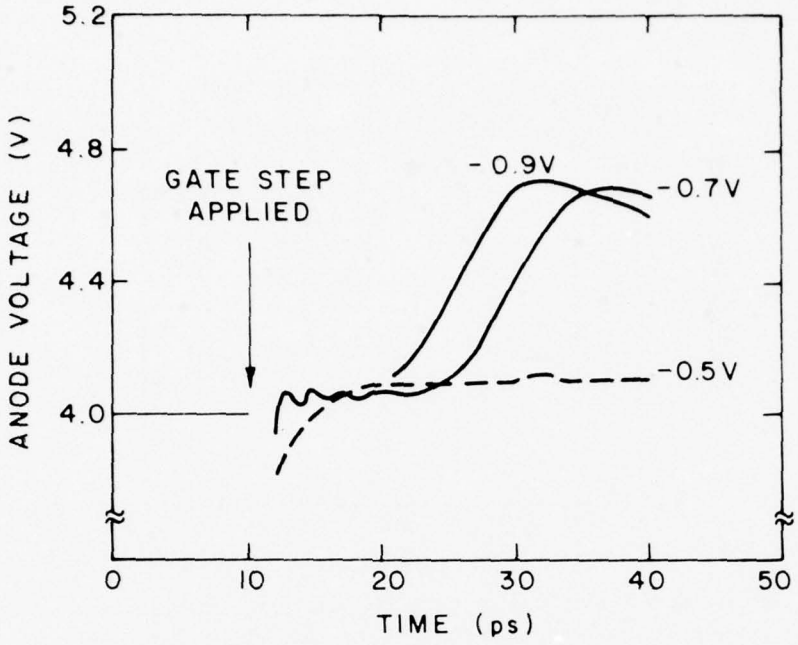


Figure 24. Anode voltage as a function of time for a gate-triggered TELD with WR_A = 5000 Ω-μm.

formation occurring under the gate. However, for these parameters a mature domain does not form and the anode voltage returns to 4 V at t $\approx$ 60 ps, as shown in Fig. 25.

The minimum value of WR_A found necessary for proper gate triggering of domains was found to be 8000 Ω-μm. Figure 26 shows the anode pulse computed for this case with V_G = 0.9 V. The anode pulse height is about 0.6 V except for an initial peak of 1.2 V prior to stable domain formation. The anode voltage returns to slightly above 4 V when the domain is collected at the anode. If the gate pulse is lengthened (dashed line in Fig. 26), then no major change in anode pulse occurs except for the initiation of a new domain after collection of the first one.

Figure 26 shows that the propagation delay is less than 20 ps for this device and that a stable domain is formed about 35 ps after the gate is pulsed. However, there is no gain achieved here. The gate pulse height can be reduced to 0.5 V and will still produce the 0.6 V output pulse. Thus, 1.2 voltage gain is achievable. Figure 27 shows the lead edge of the output anode pulse for gate pulse heights of 0.4, 0.5, and 0.9 V. Notice that the reduction of the gate

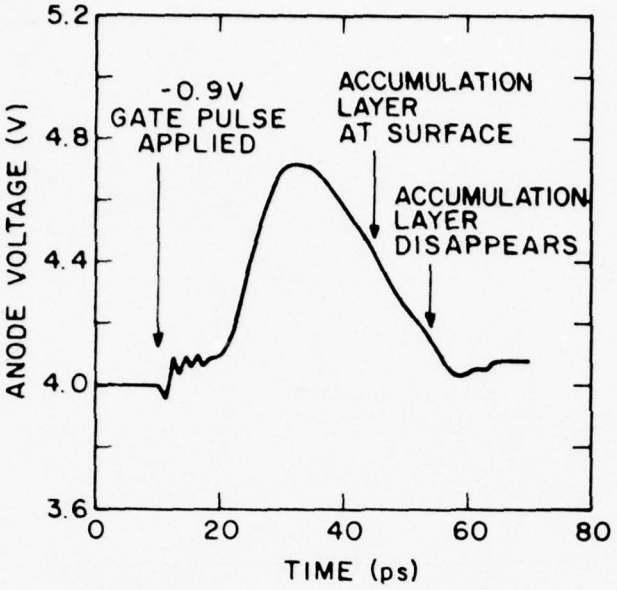


Figure 25. Anode voltage as a function of time for a gate-triggered TELD with WR_A = 5000 Ω-μm and a 0.9-V gate pulse applied at 10 ps.

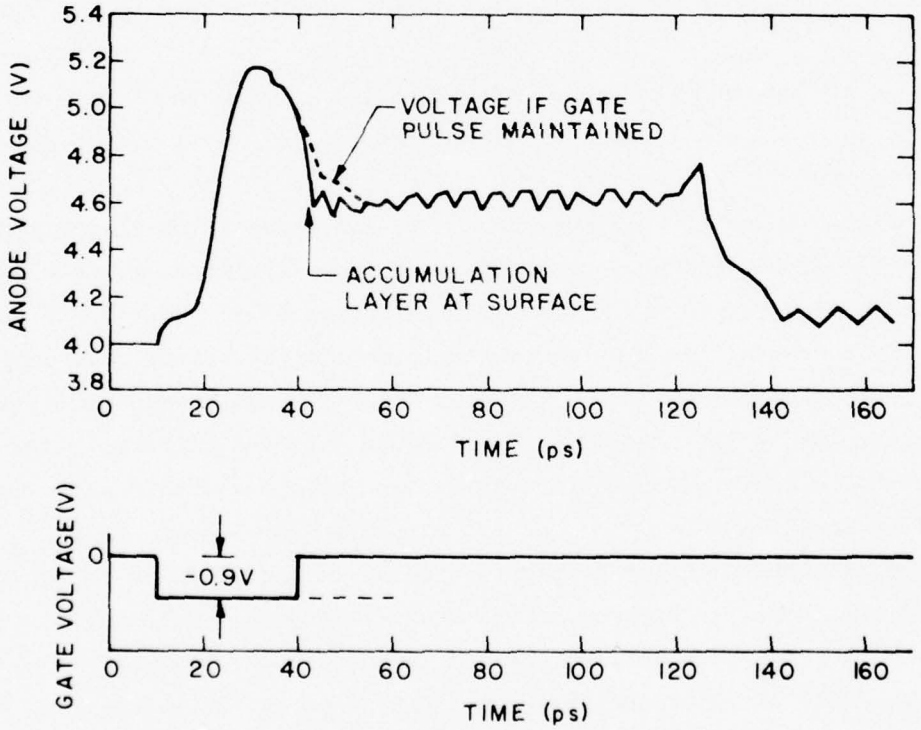


Figure 26. Gate voltage (lower figure) and resulting anode voltage (upper figure) as a function of time for the gate-triggered TELD with WR_A = 8000 Ω-μm.

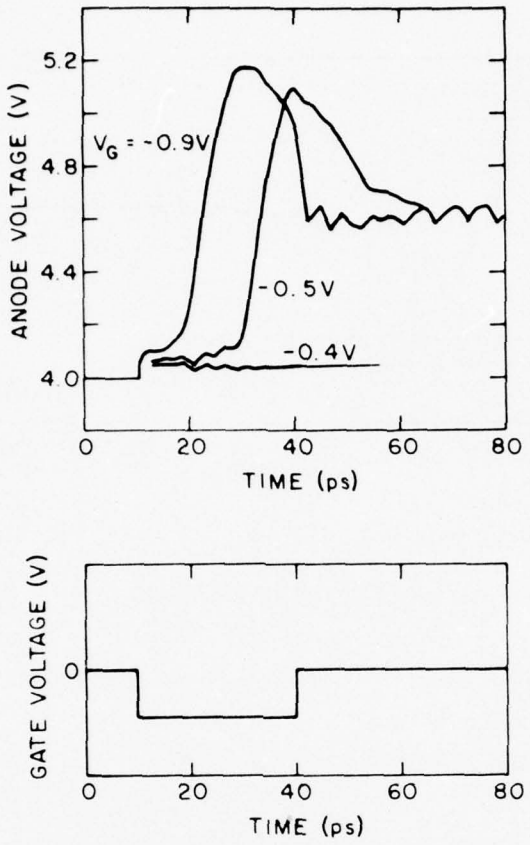


Figure 27. Gate voltage (lower figure) and resulting anode voltage (upper figure), for different values of gate voltage, as a function of time for the gate-triggered TELD with WR_A = 8000 Ω-μm.

pulse to 0.5 V causes an increase in the propagation delay. Figure 27 shows the threshold behavior, since a domain will not form for gate pulse heights of 0.4 V or less.

The results with only a cathode resistor will now be discussed. Simulation with WR_C<8000 Ω-μm again failed to produce proper domain triggering. When WR_C = 8000 Ω-μm and gate pulse height = 0.9 V, a domain can be triggered and will travel toward the anode as long as the negative gate signal is maintained. If the gate is returned to 0 V, the traveling domain is destroyed and the cathode voltage transient causes forward biasing to occur at the gate. The gate pulse can be removed when the domain is collected at the anode. Figure 28 shows the

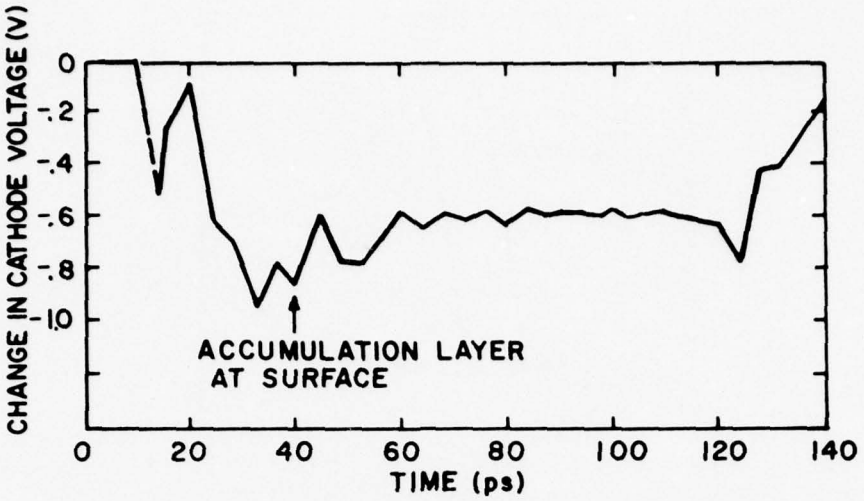


Figure 28. Change in cathode voltage as a function of time for the gate-triggered TELD with WR_C = 8000 μm and a 0.9-V pulse applied at t = 10 ps.

change in cathode voltage for this case. Again, after an initial large peak, a pulse height of 0.6 V results.

When the gate pulse height is reduced to 0.6 V, the cathode pulse is of about the same magnitude as that shown in Fig. 28, but is delayed by approximately another 8 ps. There is a unity gain condition. No cathode pulse results for a gate pulse height of 0.4 V, since this is below the device's threshold.

Note that for the device parameters being simulated, $WR_D \approx 4000$ Ω-μm, where R_D is the low-field resistance of the device. These simulations show that, for proper domain triggering, the load resistance should be about twice the device's low-field resistance. This is consistent with both first-order analytical calculations and experimental results.

D. SUMMARY

Two different lengths of three-terminal TELDs were studied. The current-voltage characteristic of each showed saturation near threshold, and no sustaining voltage less than threshold. The percentage current drop was significantly less than the previously considered two-terminal devices (i.e., for similar values of μ). A reduction in epi-layer thickness reduced the current drop much more

than did a reduction in N_D. Dipole domains were shown to form at the anode edge of the gate.

The switching properties of the shorter (13 μ) TELD were investigated for operation with either anode or cathode load resistances. A minimum value of load resistance about twice the device's low-field resistance was found necessary in each case for the proper gate triggering of domains. Threshold behavior for an applied gate voltage was shown in each case. The gate pulse must be maintained for proper operation with cathode resistance, but not for operations with anode resistance. A delay of approximately 30 ps was obtained for the case of anode output with gain.

Almost all of these results are in agreement with experimental observations. However, cases with higher doping values should be simulated, since such values are used in the experimental devices. This requires much more computing time, since the time step must be reduced. Efforts expended thus far were mainly intended to prove the analysis physically valid. Future efforts should be directed toward design improvement in these devices.

V. TRANSVERSE-DOMAIN-SPREADING (TDS) DEVICES

A. INTRODUCTION

A significant development in TELD research was the recognition that the transverse-spreading velocity of the TE domain was 30 times that of its longitudinal velocity [23]. This property was utilized to develop a carry generator for a full adder that had a propagation delay of 12.5 ps per carry bit [24]. This achievement indicates that the development of TED logic may have a revolutionary impact on the field of multigigabit-rate signal processing.

The high-speed transverse-domain-spreading phenomenon used in the carry generator offers the potential of minimizing the number of devices and interconnections required for an ultrahigh-speed logic system. It may be possible to utilize this effect to essentially "guide" information flow downstream for further processing. This implies that a high-field domain, once it is generated, may be used to perform more than one logic operation without having to derive an output voltage and to charge the input capacitance of another TELD via an interconnect transmission line. A systematic use of two-dimensional domain-spreading effects may allow the development of logic system architectures that will fully exploit the high-speed potential of the transferred electron effect.

Figure 29 shows a representation TED logic device that utilizes transverse-domain-spreading effects. Suzuki et al. [7] and Goto et al. [25] have analyzed such TDS devices by using a two-dimensional model for the X-Y plane while assuming no variation in the Z direction. The assumptions and equations used for the solution in the X-Y plane are very similar to those employed for the X-Z plane, except for the specific boundary conditions.

Two designs of exclusive-OR circuits based on a TDS device and a TELD will be described. Several design problems will be discussed. All of the TDS

---

23. K. Tomizowa, M. Kawasheina and S. Kataoka, "New Logic Functional Device Using Transverse Spreading of a High-Field Domain in n-type GaAs," Electron. Lett. 7, 239 (1971).
24. T. Nakamura et al., "Picosecond Gunn-Effect Carry Generator for Binary Adders," Int. Solid State Circuits Conf. Digest, Philadelphia, Pa., Feb. 1975, pp. 166-167.
25. G. Goto, T. Nakamura, S. Hasuo, K. Kayetani, and T. Isobe, "Gun Effect Logic Device Using Transverse Extension of a High Field Domain," IEEE Trans. Electron Devices ED-23(1), 21-27 (1976).

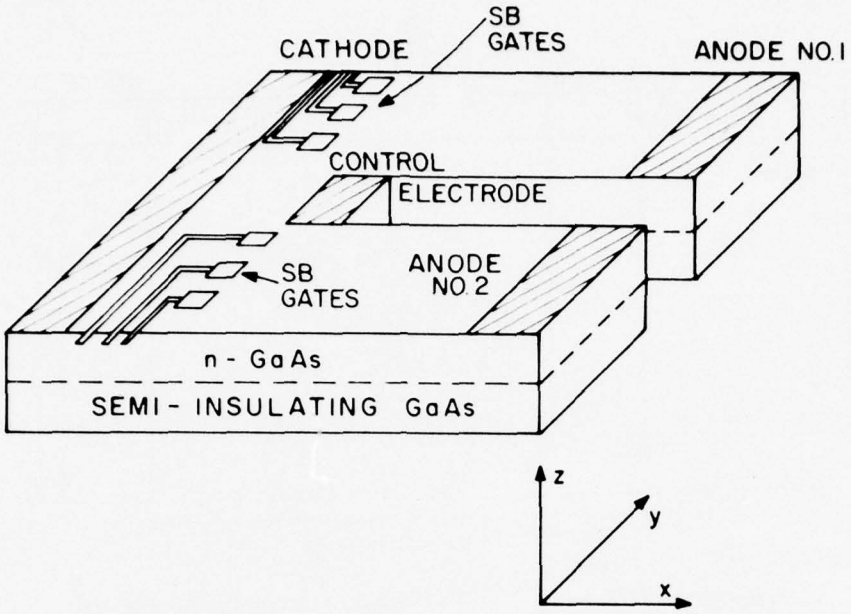


Figure 29. Schematic representation of a TELD utilizing transverse-domain-spreading effects.

designs are preliminary. Considerably more study will be needed to develop an optimized design for the exclusive-OR circuit.

B. FUNDAMENTAL CHARGE-SPREADING VELOCITY

A simple model was used to investigate a number of fundamental properties of domains. Figure 30 shows the surface of a simple planar device with a Schottky-barrier gate on one side. The surface is parallel to the X-Y plane of Fig. 29. The device was biased with $V_1 = 0$, $V_2 = 0$, $V_3 = 3\ V_1$ and a dc solution was found. The following parameters for the simulation are assumed:

$\mu = 5500\ cm^2/V\text{-}s$

$N_D = 2 \times 10^{15}/cm^3$

Diffusion coefficient = $200\ cm^2/s$

Mesh spacing = $0.5\ \mu m$

Time step = $0.4\ ps$

The anode voltage was then suddenly raised to 6 V to cause domain formation. The electric field values along a line from anode to cathode (longitudinal

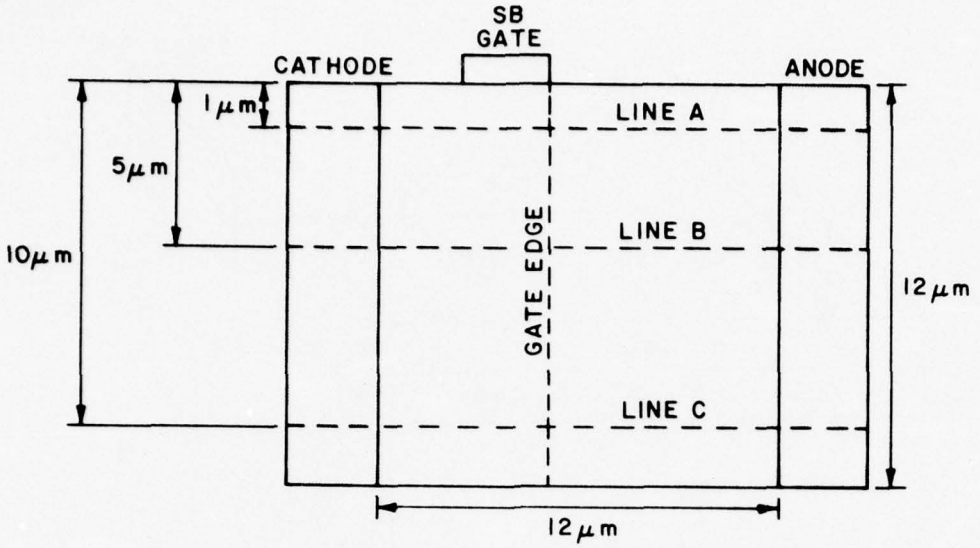


Figure 30. TDS-device model used for computation of domain-spreading properties (X-Y plane).

direction) were then evaluated at various times and at various distances (transverse direction) from the Schottky gate. Figure 30 shows the three lines used for computation.

Figure 31 shows the results of the simulation. The time parameter shown is the time elapsed after switching of the anode voltage from 3 to 6 V. A domain forms within 8 ps under the gate edge; domain formation 5 and 10 μm away follows very shortly thereafter. At 20 ps, a nearly mature domain exists across the full width of the device and travels to the anode. At line C, the domain has traveled about 3 μm toward the anode at 20 ps, whereas at line A it has traveled about 1 μm. Thus average longitudinal velocity is approximately

$$\frac{2\ \mu m}{20\ ps} = 1 \times 10^{7}\ cm/s$$

The transverse-spreading velocity is much larger than this. If one follows the spreading of charge density of N_D plus 10% along the gate-edge line shown

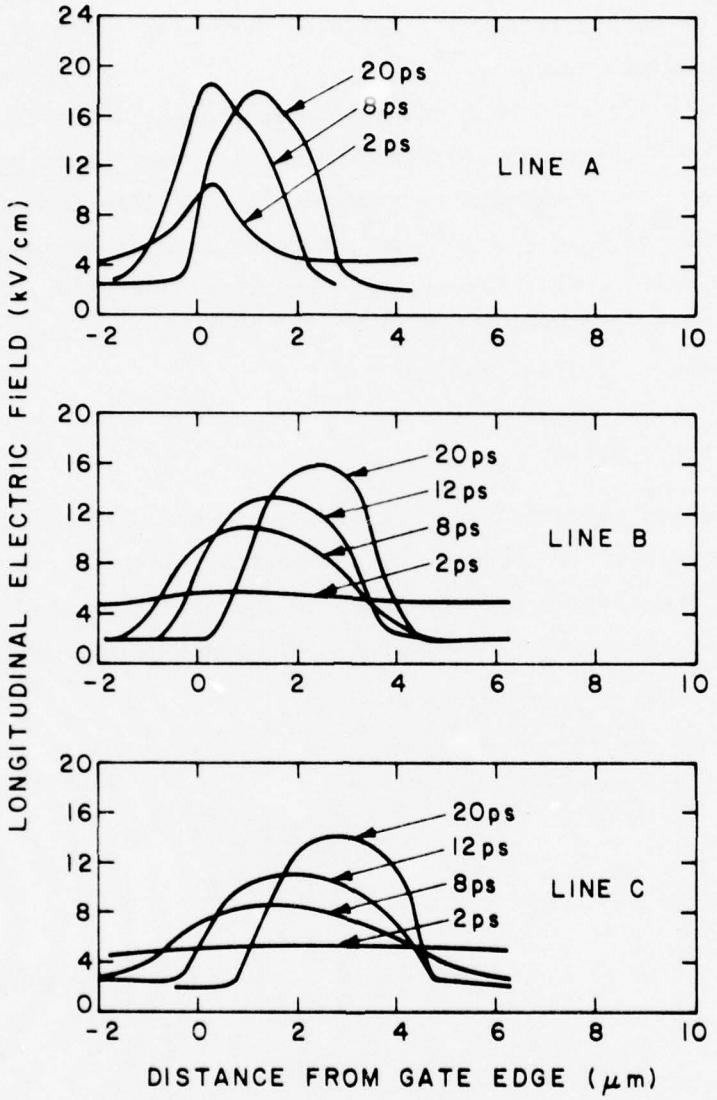


Figure 31. Electric field vs a function of distance from the gate edge and time for the device of Fig. 30.

in Fig. 30, then the charge is seen to spread 10 μm transversely in 4 ps, a velocity approximately equivalent to

$$\frac{10\ \mu m}{4\ ps} = 2.5 \times 10^8\ cm/s$$

In this simple case, the transverse (charge) spreading velocity is about 25 times the longitudinal velocity.

Suzuki et al. [7] show that the lateral-spreading velocity of space charge depends upon the donor density, the excess domain voltage, the width of the domain, and the proximity to a boundary. For less than 10 μm from the domain in material of $N_D \approx 2 \times 10^{15}/cm^3$, they estimate a maximum spreading velocity of 1.9×10^8 cm/s. The presence of other electrodes, less domain voltage, and more complicated boundaries will be seen to reduce the transverse-spreading velocity to smaller values.

C. EXCLUSIVE-OR CIRCUIT

Figure 32 shows an exclusive-OR gate constructed with a TDS device. Either A or B may initiate a domain in the device. If both do, then the three-terminal TELD applies a low voltage at the gate (between the anodes) and transverse-domain spreading is inhibited. An output results only if $A\bar{B} + \bar{A}B = 1$.

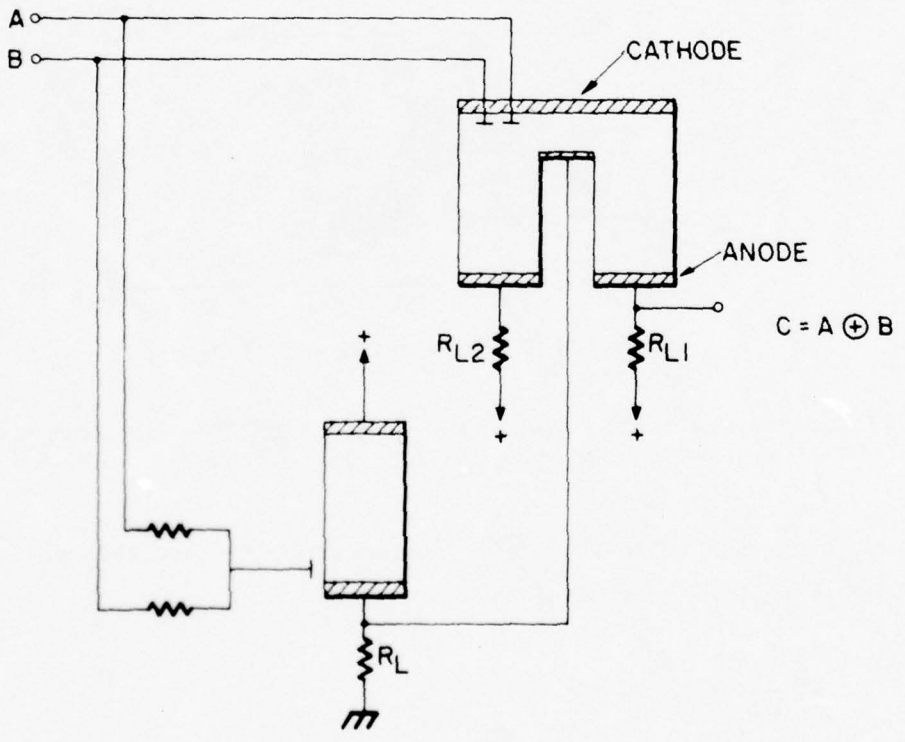


Figure 32. Exclusive-OR circuit based on TDS device.

This type of TDS device has been simulated and studied by means of the computer program for transient analysis. Several calculations will be presented here.

1. Simulation of a Small Device

The geometry of a device analyzed is shown in Fig. 33. It is similar to the carry generator described by T. Nakamura et al. [24]. A domain is initiated by means of a depletion notch (50% N_D) located 2 μm from the cathode and in line with anode no. 1 only. This simulates surface triggering of a domain by a Schottky-barrier gate. After the anode voltages are switched on, a high-field domain forms rapidly at the doping notch. The charge accumulation and depletion regions propagate transversely until a domain exists across the full width of the device.

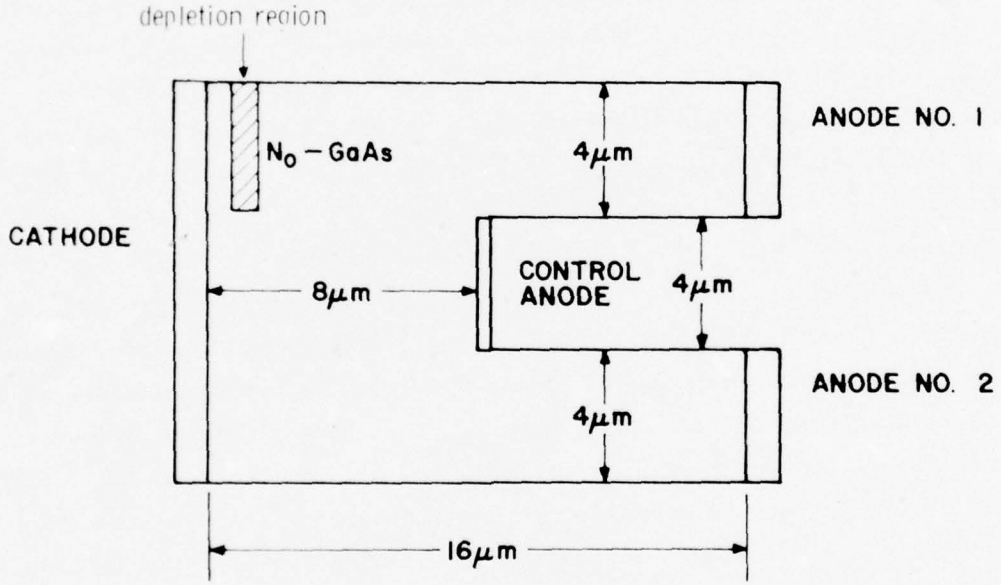


Figure 33. Geometry of a TDS device.

Computations were based on the dimensions shown in Fig. 31 and the following parameters:

Anode no. 1 voltage	= 6 V
Anode no. 2 voltage	= 5 V
Mesh spacing	= 0.5
Diffusion coefficient	= 200 cm^2/s
Donor density	= $2 \times 10^{15}/cm^3$
Time step	= 0.4 ps
Low-field electron mobility	= 5500 $cm^2/V\text{-}s$

Figure 34 shows values of the electric field along a line from the cathode to the center of anode no. 2 for V_G = 3 V. The transverse-spreading velocity of excess charge is approximately 1.2×10^8 cm/s. Note how the domain builds up and propagates. First a mature domain is formed at 20 ps; it then propagates toward anode no. 2. At 60 ps the domain has entered the arm of the device containing anode no. 2. When calculations are repeated for V_G = 2.3 V, the electric field along this line remains below threshold for all time values.

The current to anode no. 2 (the output) can be calculated for various values of control-anode voltage, V_G. Figure 35 shows this current for V_G = 3 V, where a domain has spread across the device and for V_G = 2.3 V, where transverse-domain spreading is inhibited. No current change occurs for the latter case.

The current drop for V_G = 3 V consists of an initial value produced by the lower electric field in the anode region, plus a drop resulting from domain formation. The current drop due to domain formation is not significant until about 20 ps later when the domain is mature. The maximum current drop does not occur until about 60 ps; the reason for this can be deduced from Fig. 34.

Most of the current to anode no. 2 is drift current that is proportional to the electric field. Figure 34 shows that the electric field in the anode arm (i.e., for a distance > 8 μm) remains about 2.44 kV/cm until the domain has entered the anode arm; then it becomes lower (2.09 kV/cm at 60 ps). Thus, the additional 40 ps delay for maximum current drop is related to the time it takes the domain to enter the anode arm. This is consistent since between t = 20 and t = 60 ps the domain travels about 4 μm, or at a velocity of 4 μm/40 ps $\approx 1 \times 10^7$ cm/s. For faster output response, it would therefore be best to reduce the distance to the anode arm.

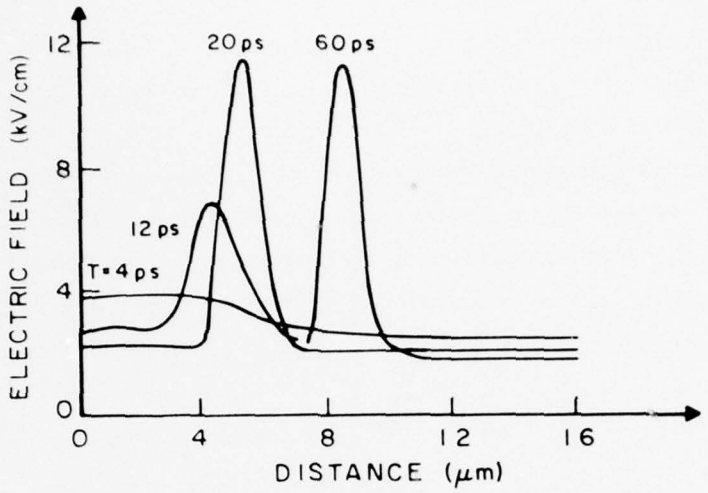


Figure 34. Results from the model of Fig. 33 for electric field as a function of distance from the cathode and at the center of anode no. 2.

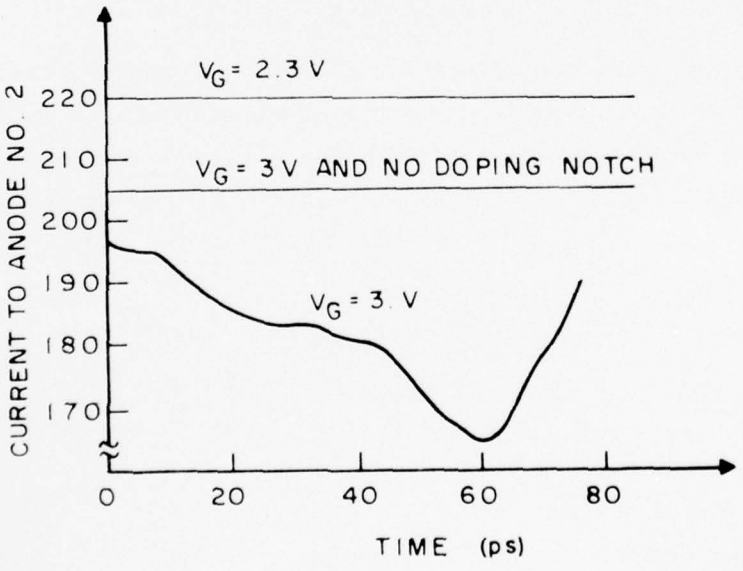


Figure 35. Results from the model of Fig. 33 for current to anode no. 2 as a function of time.

Figure 35 also shows that in the absence of a doping notch and at V_G = 3 V, no current drop occurs in anode number 2. This is equivalent to the condition of no gate (input) triggering.

The impedance presented by the control electrode is important to the operation of this device. The calculations show that this region behaves like a two-terminal device. That is, as V_G is increased to 3 V, a current drop occurs. The current to the gate is always less than the current to either anode, but the impedance of the gate is roughly the same as that of either anode. This is quite undesirable.

A device with control anode width of 2 μm was simulated and found to work not as well. The higher electric fields generated near the inner corners of the control anode lead to domain formation in these regions. This tendency is still present in the device of Fig. 33. The problem appears to be less troublesome if the doping is increased at the contact (of the control anode) and if the geometry of the corners is changed, as was done by Goto et al. [25]. These researchers, however, observed that a short cathode-to-gate separation of 7.6 μm and/or a narrow width of 4 μm produced an uncontrollable operation. A study of a device of larger dimensions is discussed below.

2. Simulation of a Larger Device

Figure 36 shows a similar device, in which the anode-cathode spacings are the same as before, but the transverse dimensions have been increased. To produce higher impedance, the control-anode width was not increased as much as the transverse dimensions. The following parameters are assumed for computations:

V_1	= 6 V
V_2	= 5.6 V
V_G	= 2.5 and 3 V
R_2	= 0 Ω
Mesh spacing	= 1 μm
Diffusion coefficient	= 200 cm^2/s
Donor density	= 2 x $10^{15}/cm^3$
Time step	= 0.8 ps
Low-field electron mobility	= 5500 $cm^2/V\text{-}s$

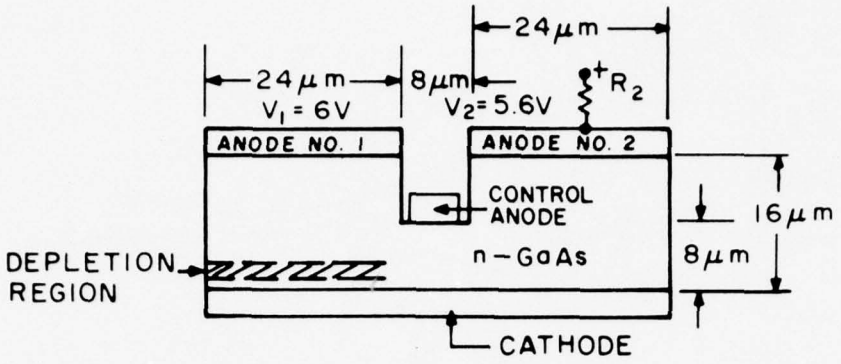


Figure 36. The geometry of a large device.

Figure 37 shows the currents to anode no. 2 and 1, respectively, for snap-on of the voltages in the presence of a depletion region. A domain forms at the depletion region and causes an immediate current drop for anode no. 1 for both values of V_G. The transverse spreading is inhibited for V_G = 2.5 V, but not for V_G = 3 V. Thus, a current drop occurs in anode no. 2 for V_G = 3 V, but only after about 60 ps. This delay is due mostly to the time required for domain growth and travel. It takes 48 ps for a mature domain to grow opposite anode no. 2, and 56 ps for it to reach the arm containing anode no. 2. The transverse-spreading velocity here is low (about 0.7×10^8 cm/s). In combination with the larger distances to travel this results in excessive delay for an output signal.

For the case of R_2 = 0, it was found that anode no. 2 must be near threshold or the resulting current drop will be very small. Thus, V_2 = 5.6 V, rather than 5.0 V, must be used here. However, V_G cannot be allowed to go much below 2.5 V or threshold electric field (due to V_2-V_G) is exceeded in the anode region. This difficulty is partially overcome by use of the anode resistor (R_2). V_2 may then be set below 5.6 V, reducing the anode field; when current drop occurs, the anode voltage will rise. In fact, as a result of the current drop, the anode resistor permits V_2 to increase above 6 V at 48 ps. The domain grows faster in this case but, as seen in Fig. 37, there is only a small decrease in delay time.

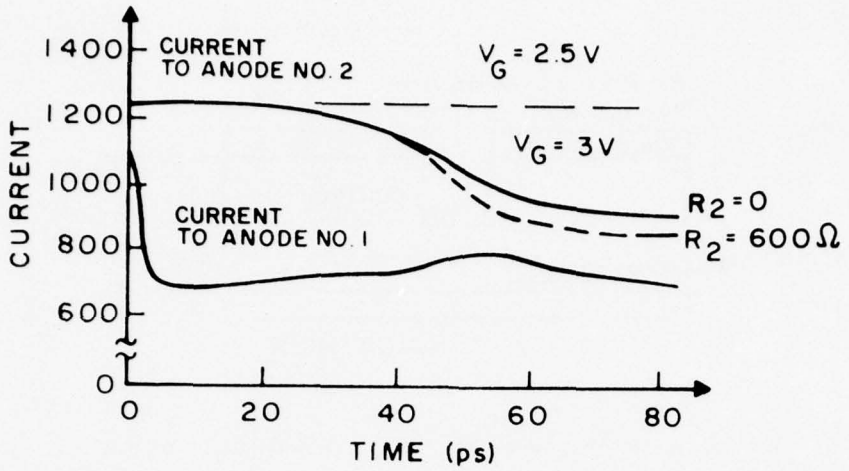


Figure 37. The anode currents as a function of time for the model of Fig. 36.

With a 10-μm-thick epi-layer the following operating parameters apply:

Current to anode no. 2 for a V_G of 2.5 V	= 12.4 mA
Current drop in anode no. 2 for a V_G of 3.0 V	= 3 mA
Maximum control-anode current for a V_G of 2.5 V	= 2 mA
Current drop for anode no. 1	= 5 mA
V_2 change for V_G change from 3 to 2.5 V:	
for R_2 = 600 Ω	= +2.1 V
for R_2 = 300 Ω	= +0.9 V

When the impedance of the control anode from its maximum current is estimated, an impedance about three times the impedance of either anode is obtained. This result was produced by the choice of a narrow width.

D. CAPACITIVE ELECTRODE OUTPUT

The delay in the output signal may be reduced by the use of a capacitive electrode in place of the second anode. This electrode can be positioned much closer to the cathode; the need for the domain to enter the anode arm before output occurs is thereby eliminated.

Mause [26] has shown that the capacitive electrode can provide an output voltage pulse of sufficient magnitude for triggering subsequent TE logic devices. This electrode is insulated from the channel by a sputtered SiO_2 layer and merely samples the channel potential beneath it. In general, for an electrode between anode and the domain, capacitive electrodes produce a positive pulse when the domain forms (because the potential rises); this changes to a negative pulse when the domain passes under it (and the potential is lowered). Thus both positive and negative outputs are available. The positive output, however, has the least time delay.

The closest an electrode could be put near the cathode for the previous two devices is 6 μm, since Fig. 34 shows the domain to be mature at this position. Assume an electrode of 4-μm width is placed 6 μm from the cathode and opposite anode no. 2 of the device in Fig. 33. If the electrode is narrow, say 0.5 μm, the output voltage may be estimated by use of the previous computations of potential. Figure 38 shows these results. A positive pulse of about 0.75 V occurs with about 20 ps delay for the case of V_G = 3 V, as compared to the case of V_G = 2.3 V. The negative pulse is delayed about 40 ps and has a value of about 0.36 V. Because of the shorter delay and larger output signal, the positive output pulse would be preferred, provided a positive pulse can be used in the following stage (as, for example, with an FET-triggered TED). The 20-ps delay represents a significant improvement over the 60-ps delay illustrated in Fig. 35. A similar improvement can be obtained for the device of Fig. 36.

E. DOMAIN CONTROL WITH A SCHOTTKY-BARRIER GATE

Figure 39 is a diagram of a comb TELD. The comb has two sets of "teeth." The long teeth correspond to sections in which domains propagate and output voltage can be extracted. The other set of teeth is used to control the electric-field profile to either permit or inhibit domain-transverse spreading. The first set of teeth is identical to TELDs with capacitive pickoff, as discussed in the previous section. The design considerations for the control section are described below.

---

26. K. Mause, "Delay Structures with Planar Gunn Devices," Electron. Lett. 11, 408-409 (1975).

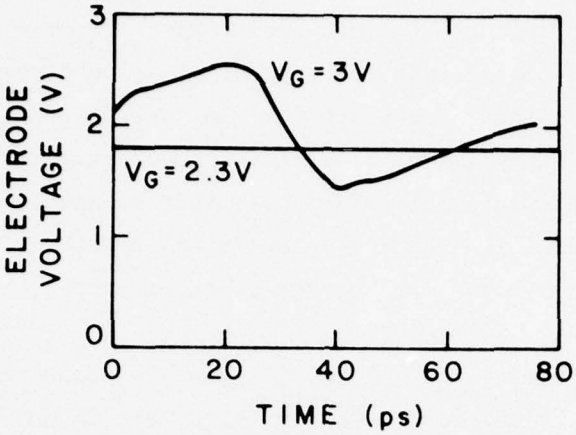


Figure 38. The voltage at a capacitive electrode as a function of time for V_G = 2.3 and 3 V; the electrode is placed 6 μm from the cathode at the TDS device of Fig. 33.

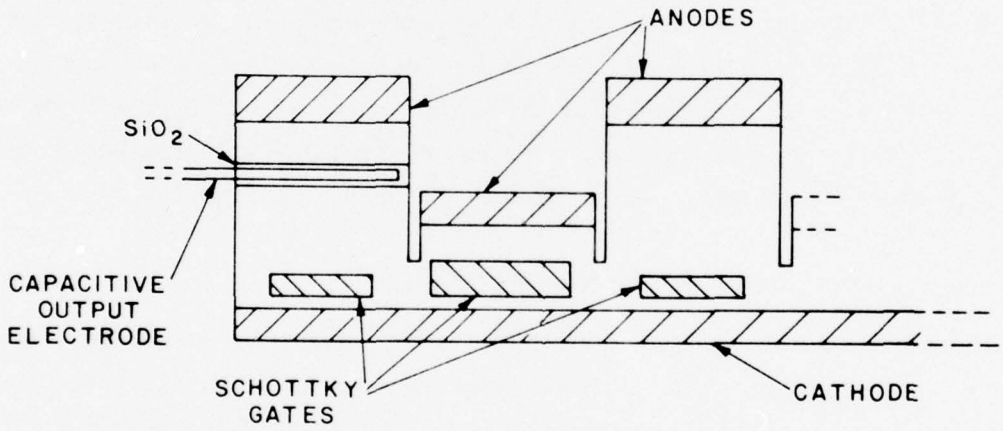


Figure 39. Comb-shaped TELD with Schottky control contacts.

The control section shown in Fig. 39 differs from that described in the literature [25]. This control electrode is a Schottky-barrier contact in contrast to the ohmic-control electrode described previously. The ohmic contact requires both trigger voltage and current and is not very compatible with TELDs. The Schottky contact only requires charging current and is thus more compatible with the output of TELDs.

An alternative layout of an exclusive-OR circuit uses a split-gate TELD and a comb-shaped TELD. In some respects this circuit works very differently from the one described by Nakamura et al. [24]. In our comb-shaped TELD the long sections are used to initiate domains and provide output. The short sections are used to control the domain spreading in the transverse direction. Nakamura et al. [24] used an ohmic electrode for the control electrode. For an ohmic electrode to perform the control function, a large voltage pulse capable of switching large currents is required. This produces too much constraint when the trigger pulse must be derived from another logic gate and makes it more desirable to use a Schottky gate to control domain spreading in the transverse direction. The operation of the circuit with reference to Fig. 40 is as follows: The split-gate device provides an AND output. Since the capacitive pickoff serves to provide the output, the output contains both positive and negative outputs. The positive part of the output can be treated as $\overline{X \cdot Y}$. The control sections of the comb-shaped device are biased just above domain-sustaining field and far below threshold field. When a positive signal is applied to the Schottky gate, the conducting-channel thickness under it increases and hence the electric field decreases. By a proper choice of the material parameters, the field under the Schottky gate can be decreased to a value below the domain-sustaining field; as a result it can inhibit domain spreading in the transverse direction. As the electric field under the control Schottky is far below the threshold field, a negative pulse applied to it will not nucleate domains. Thus, only when a single input is present, the domain is formed in one of the outer long sections and is steered into the central section that provides a capactive pickoff output. When both inputs are present, domains are formed in both of the outer long sections, but are inhibited from reaching the central section, so that no output occurs. Hence, an exclusive-OR function is realized in this circuit.

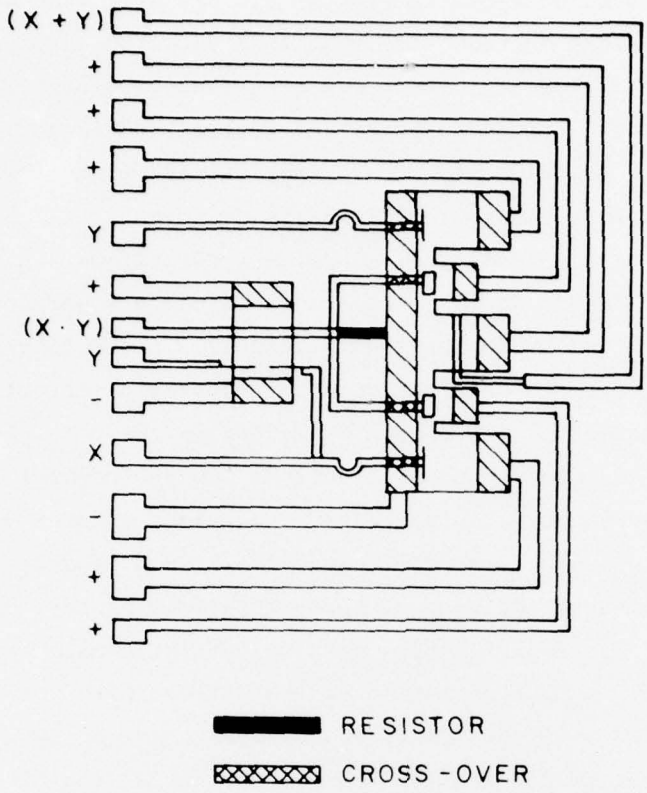


Figure 40. Alternative layout for exclusive-OR with comb-shaped device.

Preliminary simulations of this type of device were unsuccessful. Some of the problems will now be illustrated. A model for part of a larger device is shown in Fig. 41. This device contains no control electrode between anodes, but instead does contain a Schottky-barrier gate for transverse-domain control. The domain is initiated, as was done previously, with a doping notch (50% reduction) opposite anode no. 1. The effectiveness of the voltage applied to the Schottky-barrier gate in stopping the domain from reaching anode no. 2 was studied.

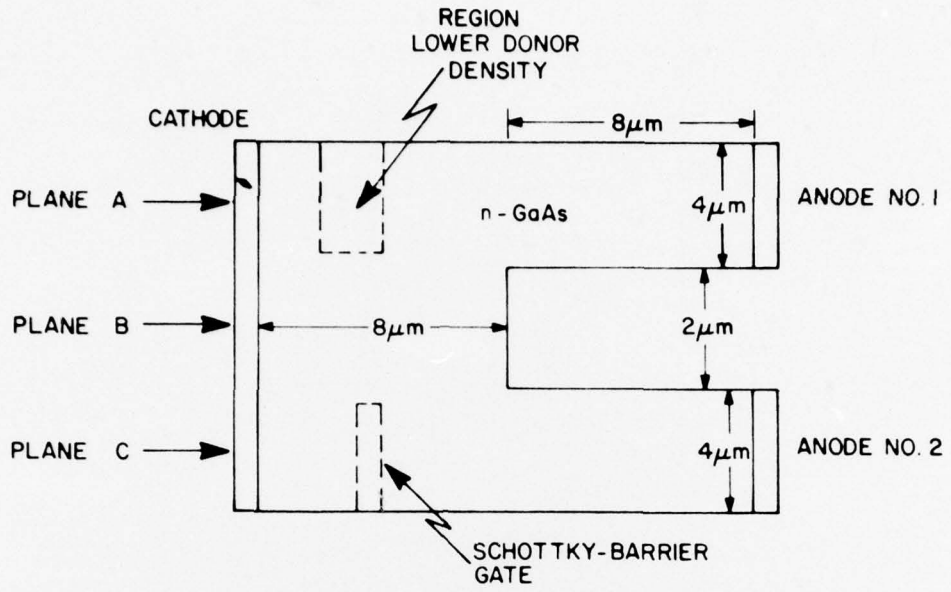


Figure 41. Geometry of a second TDS device.

The dimensions of this device are the same as those for Fig. 33, except for a narrower gap. The following parameters were used:

Anode no. 1	= 6 V
Anode no. 2	= 5 V
Donor density, N_D	= $2 \times 10^{15}/cm^3$
Diffusion coefficient	= 200 cm^2/s
Mesh spacing	= 0.5 μm
Time step	= 0.4 ps

Figures 42(a) and 42(b) show electric-field plots for planes A and C when the gate is adjusted to permit domain growth. In Fig. 41 it is seen that the domain forms at the doping notch and propagates to anode no. 1. At 80 ps the domain is well into the arm of anode no. 1. Figure 42(b) shows that no domain is present in plane C at 4 ps but that, by 8 ps, the transverse spreading has caused domain growth to take place.

Similar computations were made for the case of the Schottky-gate voltage raised by 0.2 V. Not only did this eliminate the domain from the arm of anode

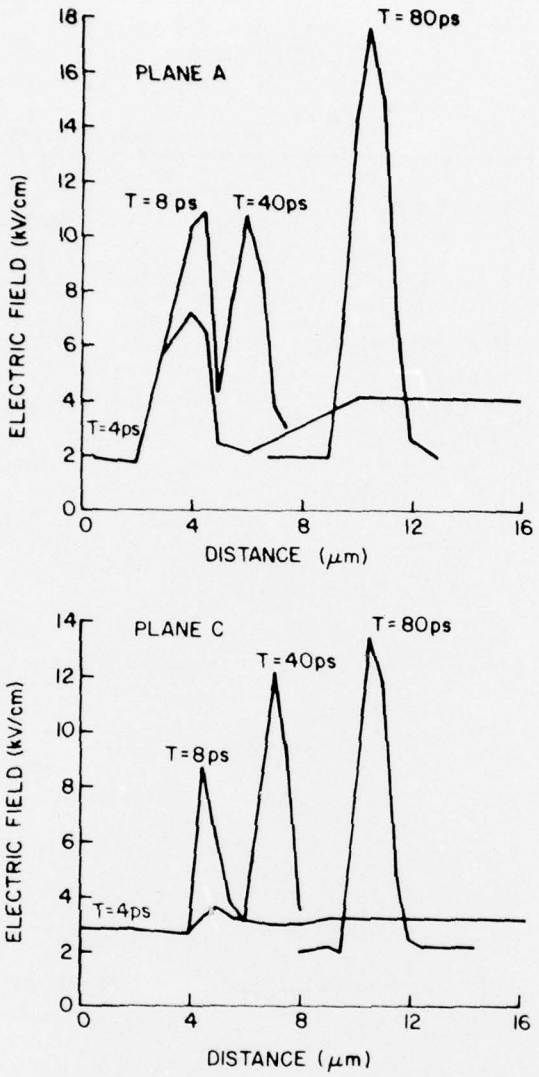


Figure 42. Electric field as a function of distance from the cathode at various times for (a) plane A and (b) plane C.

no. 2, but it also interfered with domain growth in plane A. Figure 43 shows a sample computation. At 8 ps the domain is forming properly; at 40 ps, however, it is reduced and high fields are building up again at the doping notch. This effect is undesirable and must be eliminated by design changes for proper operation.

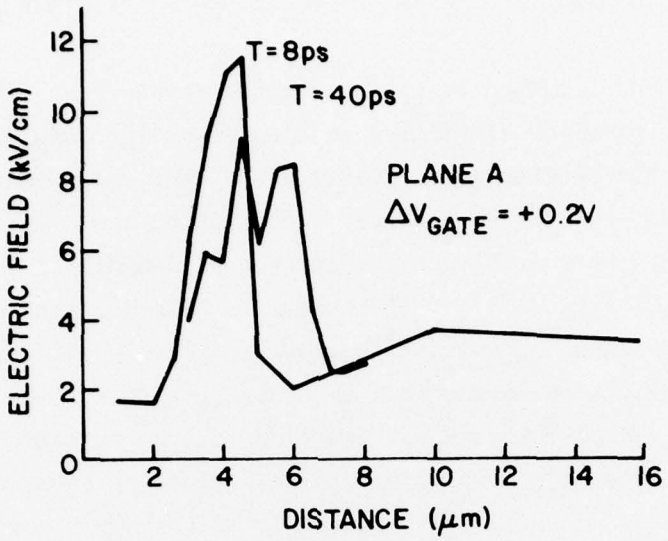


Figure 43. Electric field as a function of distance from the cathode for plane A.

VI. CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER STUDY

This study has resulted in the successful development of a program for two-dimensional transient simulation of single-carrier GaAs devices. The effects of a Schottky-barrier gate, planar ohmic contacts, planar geometry, the presence of a semi-insulating substrate, diffusion, and a nonlinear velocity-field relationship were studied. The effects of assuming a field-dependent diffusion coefficient were found to be small. A method for including the principal effects of tapering device width was also developed. Generally the mesh point spacing was chosen larger than the Debye length for more efficient program execution, even though this caused "smearing" of the depletion region. The principal restriction on the program is the neglect of intervalley transfer time. This reduces accuracy in the analysis of very small structures (of the order of a few microns) and of conditions of very high frequencies (of the order of 20 GHz).

The accuracy of the analysis was checked by verification of stable domain mode, transit-time operation in a planar two-terminal GaAs device. A drift velocity peak/valley ratio of 2.06 produced 37% current drop in a device with an $n\ell$ product of $10^{12}cm^{-2}$. When the velocity peak/valley ratio was reduced, the percentage of current drop was reduced as well.

Two different lengths of three-terminal TELDs were studied. A Schottky-barrier gate was used in each. The current-voltage characteristic of each showed saturation near threshold and no sustaining voltage less than threshold. Good transit-time operation was achieved only for an anode bias of at least 10% above threshold value. The g_m values are low in comparison to those of FETs. Dipole domains were shown to form at the anode edge of the gate.

The switching properties of the short (13 μm) TELDs were investigated for operation in a circuit with either anode or cathode resistance. For proper domain triggering by a voltage applied at the gate, a minimum value of about twice the device's low-field resistance was required in each case. It was found that the gate pulse must be maintained for proper operation with cathode resistance, but not for operation with anode resistance. Threshold behavior for an applied gate voltage was shown for each case. A delay of about 30 ps was obtained for the case of anode output with gain.

The investigation of the three-terminal devices should be continued. Larger values of N_D should be simulated, since the values assumed to date are considerably less than those typically used in real devices. Optimized designs should be developed.

Although a transverse (charge) spreading velocity as high as 2.5×10^8 cm/s was calculated in a device of simple geometry, it was shown that the comb structures studied have lower spreading velocities. In fact for devices with $N_D \approx 2 \times 10^{15}/cm^3$, it typically takes 20 ps to form a mature domain 10 μm away from the point of domain initiation. Some of this (about 8 ps) is due to the domain formation time in the material and can be reduced by using a larger N_D.

Two designs of exclusive-OR circuits were studied. Each utilized a conventional TELD with a TDS device. For this application three designs of TDS devices were analyzed. Although design guidelines have been developed, an optimized design is not yet available and will require a considerably larger effort.

For the exclusive-OR circuit, a TDS with a control anode can be made to function properly. However, the output at anode no. 2 is delayed an additional 40 ps (a total of 60 ps) due to anode-directed domain travel (to the arm of anode no. 2). This delay can be reduced by the use of smaller dimensions, and these, in turn, are possible for larger values of N_D. In addition, the control-anode width must be small enough to produce a reasonably high impedance.

The fastest output signal was shown to be achieved with a capacitive output electrode in this TDS device. The positive pulse is delayed by only 20 ps, and the negative pulse by 40 ps. This type of output must be investigated further to find its drive capabilities.

An exclusive-OR circuit based on a TDS device with Schottky-barrier-gate domain control was simulated. These conditions did not provide proper domain control. But this type of control electrode is very desirable, and further design studies should therefore be made.

It is recommended that the modeling of TDS devices be refined. Larger doping values (N_D) should be simulated, and dimensions should be reduced to decrease device delay. The use of the Schottky-barrier-gate control of domains and capacitive-output electrodes should be studied in greater detail.

APPENDIX

THE ENHANCEMENT MODE OF TELDs

A preliminary analysis of the enhancement-mode operation of three-terminal TELDs was carried out. The existence of this mode was verified with a simple device model, but no further work was done to develop an optimized device design.

Figure A-1 shows the geometry assumed for the device. These parameters were used:

Donor density, N_D	= $5 \times 10^{15}/cm^3$
Mobility, μ	= 5500 $cm^2/V\text{-}s$
Diffusion coefficient	= 200 cm^2/s
Epi-layer thickness	= 2 μm
Mesh spacing	= 0.25 μm
Time step	= 0.1 ps
Anode voltage	= 6 V

The donor density and the epi-layer thickness used each were one half of those used in the 13-μm device studied in Section IV.

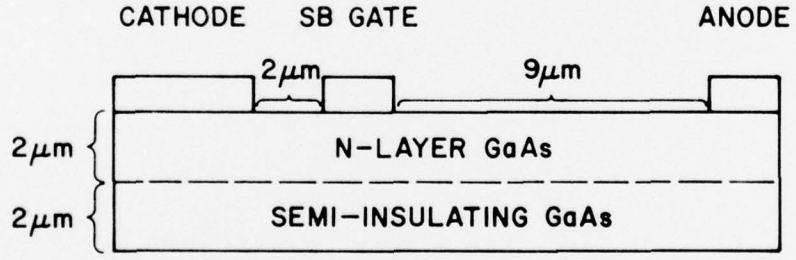


Figure A-1. Geometry of three-terminal TELD model used for the simulation of the enhancement mode.

The gate's voltage was set to -4 V, and a quiescent operating point was found. Although the anode voltage is above the usual threshold voltage, the negative gate has so cut the current flow that the voltage drop in the gate-to-anode region is insufficient to produce a domain. At time t = 0, the gate

is switched to 0 V; that is, a positive step of 4 V amplitude is applied. A high-field domain then forms and travels to the anode. Figure A-2 shows the electric field at the surface between the gate and the anode for $t < 0$ and $t = 60$ ps. The domain is obvious at $t = 60$ ps.

Figures A-3 and A-4 show the cathode and anode currents, respectively, as a function of time after the gate step at $t = 0$. A stable domain forms in about 50 ps. Transients in current are strong within the first 10 ps. These are caused by displacement currents resulting from the capacitances of the device. In fact, the difference in anode and cathode current is just equal to the displacement current of the gate.

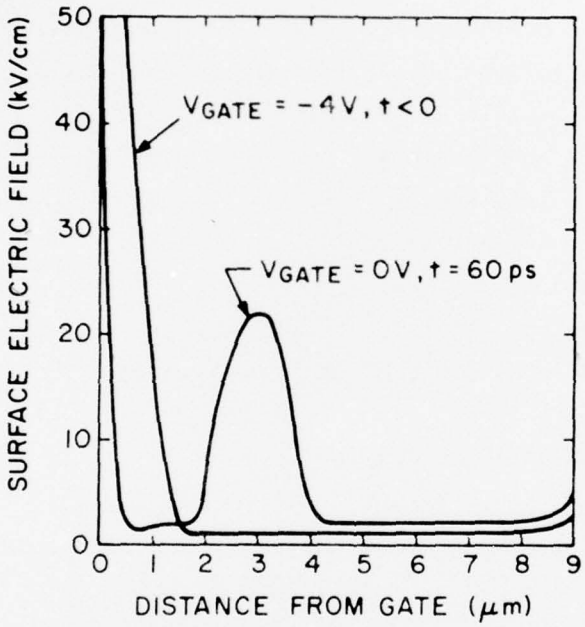


Figure A-2. Electric field along the surface as a function of distance from the gate for the device of Fig. A-1 with a gate voltage step at $t = 0$.

For this simulation, the device's current changes from 126 μA/μm at $t < 0$ to 193 μA/μm after transients have died out. This is a current change of 53%.

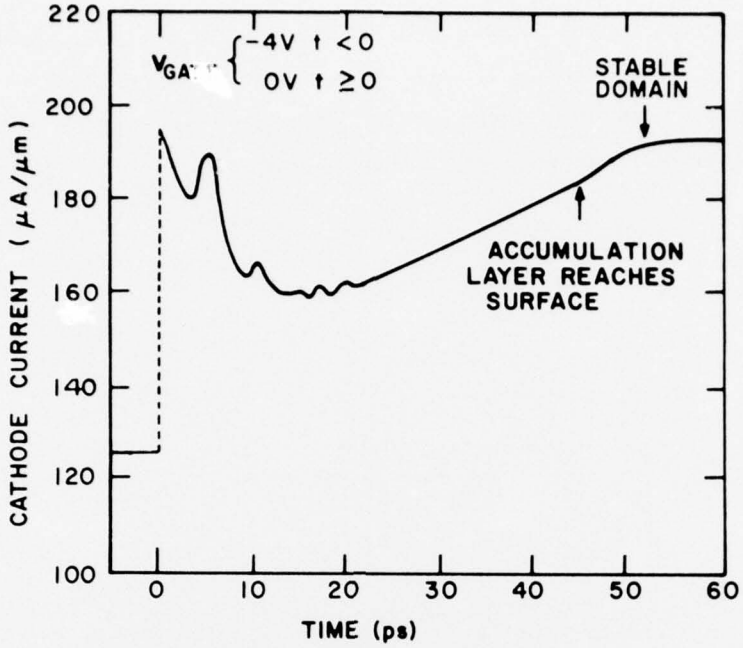


Figure A-3. Cathode current as a function of time for the device of Fig. A-1 with a gate voltage step at t = 0.

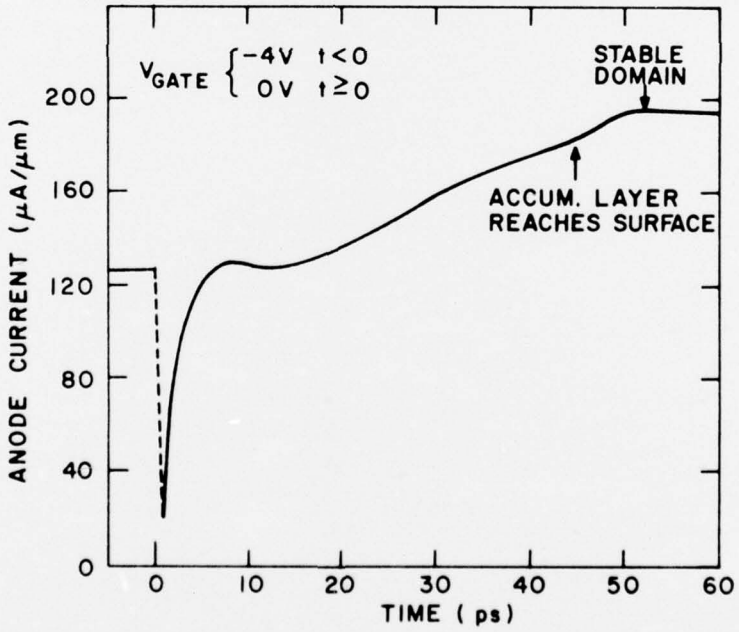


Figure A-4. Anode current as a function of time for the device of Fig. A-1 with a gate voltage step at t = 0.

In a second simulation a gate bias of -2 V with the same device parameters was found capable of providing the quiescent state. A positive 2-V step was then sufficient to turn on a domain. The current change in this case is only 26%. It again takes 50 ps to form a stable domain.

REFERENCES

1. J. W. Slotboom, "Iterative Scheme for 1- and 2-Dimensional D.C. Transistor Insulation," Electron. Lett. 5(26), 677-678 (1969).

2. P. A. Dubock, "D.C. Numerical Model for Arbitrarily Biased Bipolar Transistor in Two Dimensions," Electron. Lett. 6(3), 53-55 (1970).

3. E. J. Zaluska, P. A. Dubock, and H. A. Kemhadjian, "Practical 2-Dimensional Bipolar-Transistor Analysis Algorithm," Electron. Lett. 9(25), 599-600 (1973).

4. M. Reiser, "Two-Dimensional Analysis of Substrate Effects in Junction F.E.T.'s," Electron. Lett. 6(16), 493-494 (1970).

5. D. P. Kennedy and R. R. O'Brien, "Computer Aided Two-Dimensional Analysis of the Junction Field-Effect Transistor," IBM J. Res. Dev. 14, 95-116 (1970).

6. M. Reiser, "A Two-Dimensional Numerical FET Model for DC, AC and Large Signal Analysis," IEEE Trans. Electron Devices ED-20(1), 35-45 (1973).

7. N. Suzuki, H. Yanai, and T. Ikoma, "Simple Analysis and Computer Simulation on Lateral Spreading of Space Charge in Bulk GaAs," IEEE Trans. Electron Devices ED-19(3), 364-375 (1972).

8. G. Goto, T. Nakamura, and T. Isobe, "Two-Dimensional Domain Dynamics in a Planar Schottky-Gate Gunn-Effect Device," IEEE Trans. Electron Devices ED-22(3), 120-126 (1975).

9. K. Yamaguchi, S. Asai, and H. Kodera, "Two Dimensional Numerical Analysis of Stability Criteria of GaAs FET's," IEEE Trans. Electron Devices ED-23(12), 1283-1290 (1976).

10. C. R. Jesshope, "Numerical Solutions to the 2-Dimensional Time-Dependent Semiconductor Equations," Electron. Lett. 11(18), 431-433 (1975).

11. O. Manck and W. L. Engl. "Two-Dimensional Computer Simulation for Switching a Bipolar Transistor Out of Saturation," IEEE Trans. Electron Devices ED-22(6), 339-347 (1975).

12. J. J. Barnes, R. J. Lomax, and G. I. Haddad, "Finite-Element Simulation of GaAs MESFET's with Lateral Doping Profiles and Submicron Gates," IEEE Trans. Electron Devices ED-23(9), 1042-1048 (1976).

13. H. D. Rees, "Time Response of the High-Field Electron Distribution Function in GaAs," IBM J. Res. Dev. 13, 537-542 (1969).

14. R. W. Hockney and R. A. Warriner, "Two-Dimensional Particle Models in Semiconductor-Device Analysis," Electron. Lett. 10(23), 484-486 (1974).

15. P. E. Bauhahn and W. R. Curtice, "Monte Carlo Calculation of the Drift Velocity of Electrons in n-GaAs," Proc. IEEE 60(9), 1106-1107 (1972).

16. S. T. Jolly, L. C. Upadhyayula, H. C. Huang, and B. J. Levin, "Junction Growth Techniques for GaAs Avalanche Transit-Time Devices," U.S. Army Electronic Command, Fort Monmouth, N.J., ECOM-0308-F, 1973.

17. M. Reiser, "Large-Scale Numerical Simulation in Semiconductor Device Modelling," Computer Methods in Appl. Mech. Eng. 1, 17-38 (April 1972).

18. J. P. McKelvey, *Solid State and Semiconductor Physics* (Harper & Row, New York, 1966), pp. 332-333.

19. R. W. Hockney, "The Potential Calculation and Some Applications," Methods in Computational Physics 9, 135-211 (1970).

20. K. Blotekjaer, "Transport Equation for Electrons in Two-Valley Semiconductors," IEEE Trans. Electron Devices ED-17(1), 38-47 (1970).

21. P. M. Butcher, W. Fawcett, and W. R. Ogg, "Effect of Field Dependent Diffusions in Stable Domain Propagation in the Gunn Effect," Brit. J. Appl. Phys. 18, 755-759 (June 1967).

22. W. Fawcett and H. D. Rees, "Calculation of the Hot Electron Diffusion Rate for GaAs," Phys. Lett. 29A, 578-579 (Aug. 1969).

23. K. Tomizowa, M. Kawasheina and S. Kataoka, "New Logic Functional Device Using Transverse Spreading of a High-Field Domain in n-Type GaAs," Electron. Lett. 7, 239 (1971).

24. T. Nakamura et al., "Picosecond Gunn-Effect Carry Generator for Binary Adders," Int. Solid State Circuits Conf. Digest, Philadelphia, Pa., Feb. 1975, pp. 166-167.

25. G. Goto, T. Nakamura, S. Hasuo, K. Kayetani, and T. Isobe, "Gun Effect Logic Device Using Transverse Extension of a High Field Domain," IEEE Trans. Electron Devices ED-23(1), 21-27 (1976).

26. K. Mause, "Delay Structures with Planar Gunn Devices," Electron. Lett. 11, 408-409 (1975).

DISTRIBUTION LIST

	No. Copies
Office of Naval Research Code 427 800 North Quincy Street Arlington, Virginia 22217	4
Defense Supply Agency Defense Documentation Center Cameron Station Alexandria, Virginia 22314	12
Naval Research Laboratory 4555 Overlook Avenue, S.W. Washington, D.C. 20375	
Attn: Codes 5211	1
2627	6
Naval Ocean Systems Center Device Technology Division Code 746 San Diego, California 92152	1
Dr. H. L. Grubin United Technologies Research Center East Hartford, Connecticut 06108	1
Advisory Group on Electron Devices 201 Varick Street 9th Floor New York, New York 10014	1
Dr. G. O. Ladd Hughes Research Laboratories 3011 Malibu Canyon Road Malibu, California 90265	1
Prof. Hans L. Hartnagel Department of Electronic Engr. The University of Newcastle Upon Tyne NEI 7RU United Kingdom	1

	No. Copies
Mr. D. Claxton TRW Defense and Space Systems Group Mail Stop 1414 One Space Park Redondo Beach, California 90278	1
Dr. L. Sumney Naval Electronics Systems Command Code 3042 National Center # 1 2511 Jefferson Davis Highway Arlington, Virginia 20360	1
AFSC/AFAL Attn: Lutz Micheel Wright-Patterson Air Force Base Dayton, Ohio 45433	1
Professor Doctor Klaus Mause Forschungsinstitut der Deutschen Bundespost beim Fernmeldetechnischen Zentralamt, 6100 Darmstadt Federal Republic of Germany	1